Pigtailing of integrated optical components

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Pigtailing of Integrated Optical Components

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Preface

This thesis has been written and submitted in order to obtain the Ph.D. degree. The achievements presented are a result of a collaborative project between the company IONAS A/S and the institute COM at the Technical University of Denmark (DTU).

The project, which was performed under the Industrial Research Education Ph.D. program, was initiated in September 1997 and was finished in May 2001. The project was financed by the Danish Academy of Technical Science (ATV) and IONAS A/S.

Many people have contributed to the work of this project. First, I would like to thank my industry supervisor Lars-Ulrik Aaen Andersen at IONAS A/S for his co-operation and many fruitful discussions throughout my work. Also thanks to director Lars Rønn at IONAS A/S for starting the project and his support during the work.

At COM I would like to thank my institute supervisor and research professor Martin Kristensen for being an inspiring advisor. Also thanks to the members of the integrated lightwave circuits group for many discussions and ideas. During the design and processing phase associated professor Ole Hansen at Mikroelektronik Centret (MIC) has been very helpful with creative suggestions.

The staffs at IONAS A/S, COM, and MIC deserve thanks for providing a good frame for the work. Especially, thank to Leif S. Johansen, Søren C. Therkelsen, Karin N. Andersen, and Peter C. Nielsen. Oliver Kuhn is thanked for his suggestions and corrections for this thesis. Finally, a big hug to my husband for his support and patience during this study.

Abstract

This thesis is a part of the Ph.D. work: "Packaging of integrated optical components" carried out in collaboration between IONAS A/S and COM at the Technical University of Denmark. The work has mainly been concentrated on developing a new passive alignment method of planar waveguide components, but also a silicon motherboard for laser diode pigtailing and a Variable Optical Attenuator have been realized.

The pigtailing method consists of three major parts: a waveguide chip with alignment trenches, a fiber array with alignment trenches, and a top plate with alignment rails. The top plate aligns the waveguide chip and the fiber array with respect to each other.

A process sequence for each of the three parts has been developed. It has been shown that the additional processing steps to fabricate the alignment trenches on the waveguide chip can be applied without altering the performance of the waveguides. The fiber array carrier and the top plate are fabricated by potassium hydroxide (KOH) etching. A method to align the mask pattern to the crystal orientation of the silicon substrate has been implemented. The impact of the etch of the nitride layer, used as an etch mask in KOH, on the line widths of the critical structures has been studied. The influence of the process parameters of a RIE etch process has been investigated with respect to the etch rate uniformity. After processing the variation of the line widths of the critical structures on the fiber array carrier and the top plate is determined.

The quality of the facet of the waveguide chip has been investigated. The dicing process has been optimized to obtain a smooth facet. Furthermore, a polishing setup and procedure have been implemented.

Finally, the assembly of the pigtailing parts has been implemented and evaluated. The parts are attached by applying an adhesive. The influence of the viscosity of the adhesive has been investigated.

Resumé

Denne afhandling er en del af Ph.D.-arbejdet med titlen "Indkapsling af integrerede optiske komponenter" udført i samarbejde mellem IONAS A/S og COM på Danmarks Tekniske Universitet. Arbejdet har hovedsagelig været koncenteret omkring at udvikle en ny passiv fibermonteringsmetode af planare bølgeleder komponenter. Desuden er et silicium substrat til fibermontering af laser dioder og en variabel optisk regulator blevet implementeret.

Fibermonteringsmetoden består af tre dele: En bølgelederprøve med monterings riller, et silicium substrat med riller til optiske fibre og montering og en topplade brugt til at positionere bølgelederprøven og fibersubstratet i forhold til hinanden.

En procesfølge for hver af de tre dele er blevet udviklet. Det er vist, at de ekstra procestrin til at fremstille monteringsrillerne på bølgelederprøven ikke påvirker den optiske kvalitet af bølgelederne. Fibersubstratet og toppladen er begge produceret med kaliumhydroxyd (KOH). En metode til at positionere maskemønstret i forhold til krystalretningen af silicium substratet er blevet implementeret. Det er blevet undersøgt om ætsningen af nitrid masken, brugt som ætsemaske for KOH, har indflydelse på liniebredden af de kritiske strukturer. Procesparametrenes indflydelse på RIE-ætseprocessen er blevet undersøgt med hensyn til uniformiteten af ætseraten. Efter processering er variationerne af linebredderne på de KOH ætsede skiver blevet målt.

Kvaliteten af bølgelederfacetten er blevet undersøgt. En eksisterende savemetode er blevet optimeret for at opnå en jævn facet. Ydermere er en poleringsmetode blevet implementeret.

Endelig er fibermonteringsmetoden blevet demonstreret og evalueret. Forskellige lime er benyttet til at fiksere de tre dele. Det er blevet undersøgt om viskositeten af limen har en indflydelse på monteringen.

Contents

Chapter 1

Introduction

Communication systems today is in rapid development. The field is expanding and the capacity of the systems is continuously increased. The era of optical communication began with two important discoveries in 1970. The propagation loss in an optical fiber was decreased from around 1000 dB/km to a value of 20 dB/km for wavelengths around 1000 nm [1]. At the same time the first GaAs semiconductor laser working at room temperature was demonstrated [2]. The real break-trough came in 1987 with the development of the optical amplifier in [3]. The optical amplifier permitted optical networks to be established over longer distances.

The main motivation for moving from electronic to optical communication is the much higher information flow (bandwidth) obtainable with optics. Currently electronic networks have a capacity of 10 Gbit/sec. With silica based optical fibers the maximum bandwidth can be increased to 10 Tbit/sec. The signal processing at the end of the optical fibers has to be done optically and not by electronic components to fully exploit this capacity. The signal processing includes splitting of the signal, re-combining signals, modulation of the signal, and combining/decombining optical signals with slightly different wavelengths (WDM/DWDM). Especially, dense WDM components with 16, 32 or even more wavelengths in the 1550 nm wavelength region is important, since the transmission of multiple optical channels over the same fiber increases the capacity.

A variety of low cost components are available based on bulk optics. Bulk optics is assemblies of lenses and thin film filters in small packages terminated with optical fibers. However, as the complexity of the components increases bulk optics have some limitations. The precise alignment of the elements causes both a high cost and instability due to the possibility of misalignment.

In 1969 it was suggested by Miller to integrate the optical components in one common substrate, similar to the integration of electronics in the semiconductor industry [4]. This was the beginning of the concept of Optical Integrated Circuits (OIC's) also called planar waveguides. The planar waveguide technology is especially convenient compared to bulk optics when the complexity of the components increases. Large scale industrial fabrication of planar waveguide components is currently done a few places in the world. For example by IONAS A/S, who is the industrial collaborator within this project.

Many planar waveguide components have been realized since Miller suggested the method in 1969. Some of the components have a high level of functionality. One thing all of the components have in common is the need of having optical fibers attached to the chip. This is being done commercially a few places in the world by now. Conventional packaging is a complex assembly process with requirements for extreme alignment accuracy and package stability. The cost is dependent on the components functionality and specifications. Commonly, the pigtailing and packaging processes are responsible for 50 - 80 % of the total processing cost of a planar waveguide component. If the cost of these processes could be reduced, then the optical telecommunication would be revolutionized. Hence, in order to realize low loss and stable fiber connection, simple accurate fiber-to-waveguide alignment together with stable fiber fixing are essential.

In prior work the importance of the fiber pigtailing has been over-shadowed by the waveguide manufacture. Today it is the fiber pigtailing that precludes integrated optics from becoming a cost effective technique. The main incentive behind this project has been to develop a new method for pigtailing integrated optical components, that can be combined with standard waveguide processing. An important factor in the development of the new method has been the cost of the method.

1.1 Outline of the thesis

The thesis consists of ten chapters, including this introduction. In **chapter two** the pigtailing technologies for a laser diode is discussed. A short review of existing laser diode pigtailing methods found in the literature is given. A change to one of the methods in order to obtain a better alignment accuracy is suggested and the fabrication process presented.

In **chapter three** the fabrication process of planar waveguide components is presented. An introduction to different choice of materials and waveguide geometries are given. In this work Plasma Enhanced Chemical Vapor Deposition (PECVD) and Reactive Ion Etching (RIE) are used to deposit the glass layers and etch the waveguide structures, respectively. A brief introduction of these two plasma-assisted techniques is given. Subsequently, the fabrication process is presented step by step. Finally, the process has been implemented to fabricate a prototype of a Variable Optical Attenuator (VOA). The design of the components and the experimental results are presented.

In **chapter four** the coupling loss between an optical fiber and a planar waveguide is estimated. The coupling loss is caused by different mode profiles and misalignment between the two core regions. The estimated loss is applied to calculate a tolerance of the fiber misalignment. Finally, a short review of planar waveguide pigtailing methods found in the literature is given.

In **chapter five** the pigtailing method developed in this project is presented. The method consist of three parts: A waveguide chip with alignment trenches, a fiber array with alignment trenches, and a top plate with alignment rails. The top plate is used to position the two other parts with respect to each other. The fabrication method for

each of the three parts is presented step by step. To design the masks for the planar waveguide part some initial experiments were carried out. The results are presented and used in the masks design.

In **chapter six** the actual processing of the waveguide chip is presented. Two different etch masks for etching of the waveguide structures have been investigated. After the processing the waveguide samples have been evaluated with respect to insertion loss and polarization dependent loss.

In **chapter seven** the processing of the fiber array carrier and the top plate is discussed. Both parts are fabricated by potassium hydroxide (KOH). A method to align the mask pattern to the crystal orientation of the silicon substrate is implemented. The photolithography process is presented, especially on wafers with deep etch holes in the surface from previous steps. A nitride layer is used as an etch mask in KOH. The precision of the pigtailing method depends on the uniformity of the line width of the KOH etched structures. The etching process of the nitride mask has a large influence on the final uniformity. Two etch processes are presented and discussed: a dry RIE etch and a wet-etch. The influence of the process parameters of the RIE etch process is investigated with respect to the etch rate uniformity. Finally, measurements on the line width uniformity across the processed wafer are presented.

In **chapter eight** the post preparation of the waveguide parts is presented. To obtain a smooth facet of the waveguide chips the dicing process has been optimized. The finish of the facet can be totally smooth by polishing of the samples after dicing. A procedure for the polishing process has been developed and the results of the initial polishing experiments are evaluated.

In **chapter nine** the pigtailing of the components is discussed. The setup and procedures for mounting of the fiber array and the top plate are presented. An evaluation of the assembly process is given. The waveguide part is mounted to the fiber array and top plate. Different kinds of adhesives have been explored throughout the mounting process. The influence of the viscosity of the adhesive is investigated. The measured insertion loss of the assembly and during the gluing process is discussed.

This thesis is concluded with a summary of my conclusions in **chapter ten**.

Chapter 2

Silicon motherboard for laser diodes

The packaging of semiconductor laser chips has always presented a range of technical problems due to the sub-micrometer tolerance required to obtain optimum coupling of the small laser spot size to the larger spot size of a single mode fiber. Self-alignment technologies allow saving of packaging time and costs by reducing critical positioning and fastening steps. The purpose of studying optoelectronic packaging was to gain knowledge about different pigtailing methods and their advantages and disadvantages. The knowledge about semiconductor laser pigtailing has been used in development of the fiber-to-waveguide pigtailing method which is the main scope in this project.

In this project a silicon motherboard for laser diode packaging has been designed and fabricated. The method is based on an existing packaging technique from the literature. In section 2.1 a short review of existing pigtailing methods found in the literature is given. The fabrication process is described in appendix A.

2.1 Laser packaging methods

Several approaches to fiber attachment of laser diodes has been presented in the literature [5, 6, 7, 8, 9]. The main difference between the techniques may be characterized by the alignment of the fiber being done actively or passively. In the active alignment technique, device alignment is based on maximization of the coupled power. In the passive alignment technique, elements are aligned by using passive alignment structures or by the use of patterned alignment marks. Various combinations of active and passive alignment techniques depending on the complexity of alignments are typically used in optoelectronic packaging.

The active alignment technique is commercially applied for fiber pigtailed laser packaging [10]. The advantages of active alignment are low excess loss, good loss uniformity and high yield; however, the disadvantages of active alignment are that the alignment procedure is extremely time consuming, and cost of labor, equipment, and operating devices may be high [11].

An attractive approach to passive alignment is provided by flip-chip solder bumps [12, 13, 6]. In this technique, solder wettable pads are provided on the two surfaces to be bonded, with each pad on one of the surfaces being covered with solder. The

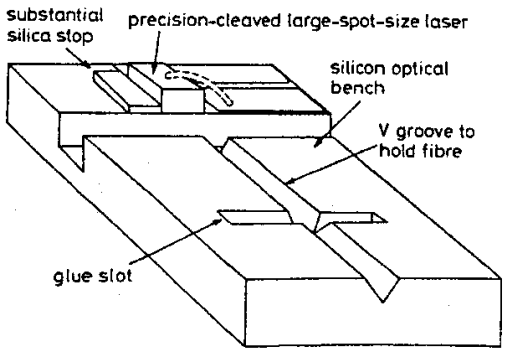


Figure 2.1: Schematic of optical silicon motherboard using V-grooves and silica standoffs for vertical alignment (from [14]).

surface tension of the molten solder pulls the corresponding solder pads into precise alignment [6]. The silicon motherboard includes anisotropically etched V-grooves for a high precision alignment of optical fiber. In front of the V-groove the bumps for flip chip mounting of the laser diodes is placed. The precision of the positioning of the solder pads and the V-grooves is determined by the precision within the photolithography alignment between the two masks.

Other chip alignment techniques use etched standoffs for vertical alignment and pedestals on the silicon providing horizontal mechanical stops together with etched notches on the chip to define the appropriate position [5, 8, 14]. An example of this is shown in figure 2.1. The main features of the silicon optical bench are V-grooves for fiber attachment and standoffs used to align the laser chips. The alignment tolerances suffer from the fact that different planes, which are produced by etching processes, have to be aligned against each other.

One approach to avoid the need for a high alignment accuracy within the photolithography is proposed by Hunziker et al. [15, 16]. A flip-chip alignment technology is used based on a silicon motherboard with etched V-grooves for the fiber array and alignment mesas, which fits into specially etched alignment trenches on the laser array chip as shown in figure 2.2. On the laser chip, alignment trenches are etched parallel to the laser array. The alignment trenches on the turned-over chip fits with alignment mesas on the silicon motherboard. Both the V-grooves for the optical fibers and the alignment mesas are etched in the same step to achieve maximum precision. Soldering provides electrical connections and fixation.

Another approach using patterned alignment marks is suggested by several groups [17, 9]. The laser diode is mounted on the silicon substrate by detecting the alignment marks on the laser diode bottom surface and the silicon substrate. To utilize this technique, accurate mark detection and precise control of the adjusting stage are required.

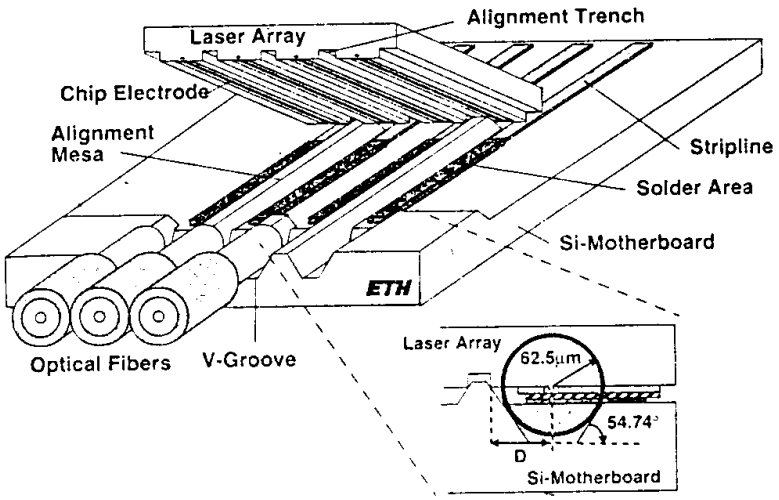


Figure 2.2: Schematic of optical self-aligned flip-chip laser array using V-grooves and alignment mesas (from [15]).

2.2 A new Silicon motherboard

In this work a silicon motherboard comparable to the method suggested by Ambrosy et al. [6] has been designed and fabricated. To avoid the need of a high alignment accuracy between the different photolithography steps the solder bumps and the V-grooves are defined within the same photolithography step. Hence, obtaining the maximum precision between the solder bump pattern and the V-grooves. The height alignment is still controlled by the height of the solder bumps.

Schematic of the fabrication method for the silicon motherboard is shown in figure 2.3. A layer of 0.3 μm thermal oxide is grown and 0.2 μm nitride is deposited on top of that. The solder pad and the V-grooves are patterned in a standard photolithography step (figure 2.3A). The mask is transferred into the nitride layer by RIE (figure 2.3B). The metal layer for the solder pads is evaporated on the substrate. The layer consist of 100 Å chromium, used as an adhesion layer, and 3000 Å gold (figure 2.3C). The metal layer on top of the resist layer is removed by a lifting process in acetone with ultrasound. The solder pads are now defined and the metal layer is also in the V-grooves (figure 2.3D). A standard photolithography process is used to cover the area of the solder pads (figure 2.3E). The gold layer in the V-grooves is etched by a iodic wet-etch. The chromium layer is etched by mixture of HNO_3, cerisulfate, and water. The layer of thermal oxide is etched by buffered hydrofluoric acid (figure 2.3F). Finally, the V-grooves are etched by a mixture of potassium hydroxide and water (figure 2.3G). A detailed process sequence is listed in appendix A.

SEM pictures of the fabricated silicon motherboard are shown in figure 2.4(a) and 2.4(b). The advantage of this processing method is that the vertical alignment does not depend on the alignment accuracy of the photolithography process. The horizontal alignment is achieved by the solder process and the width of the V-grooves. To obtain a precise width of the V-grooves the mask pattern has to be aligned to the crystal

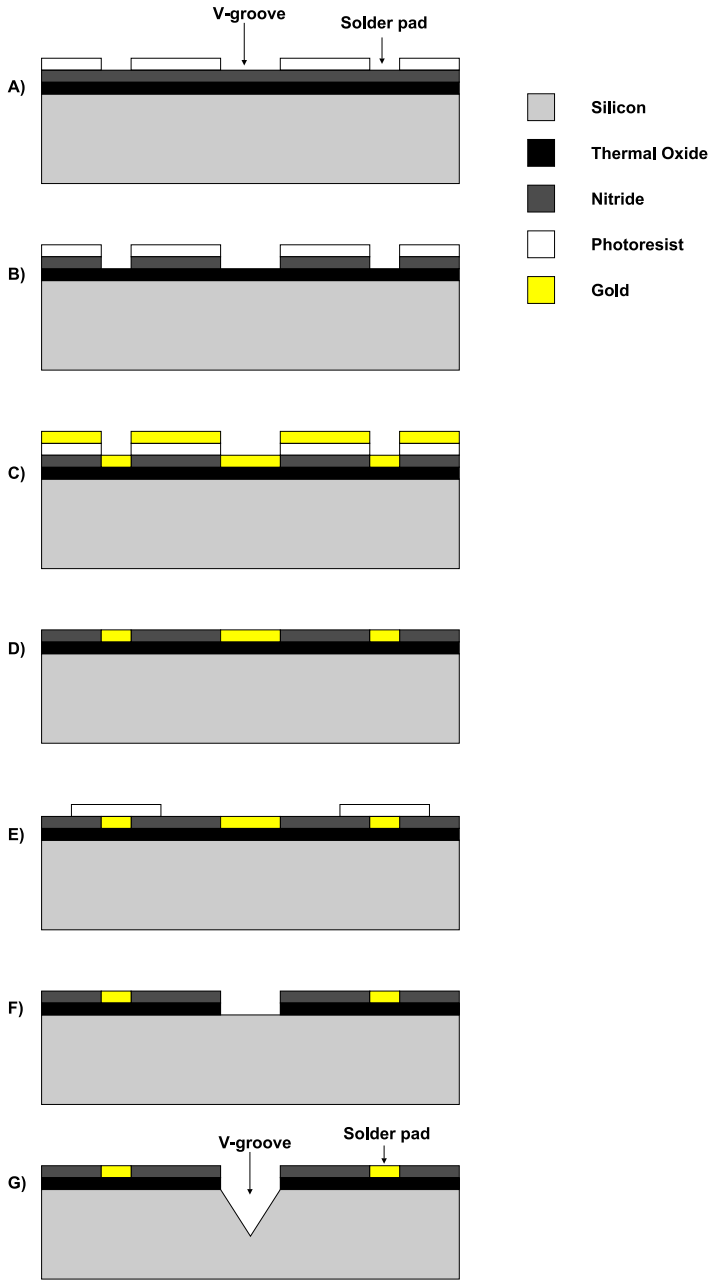
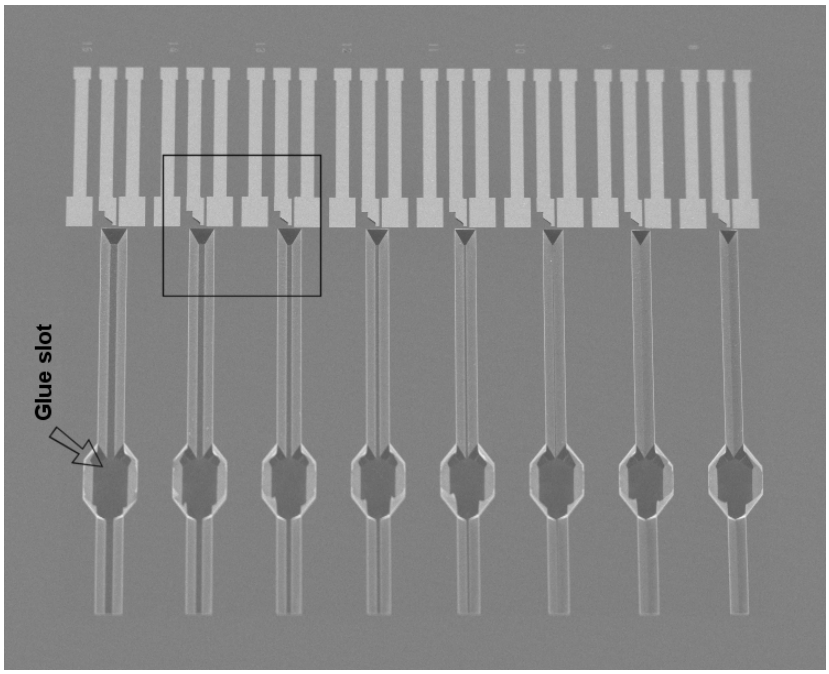
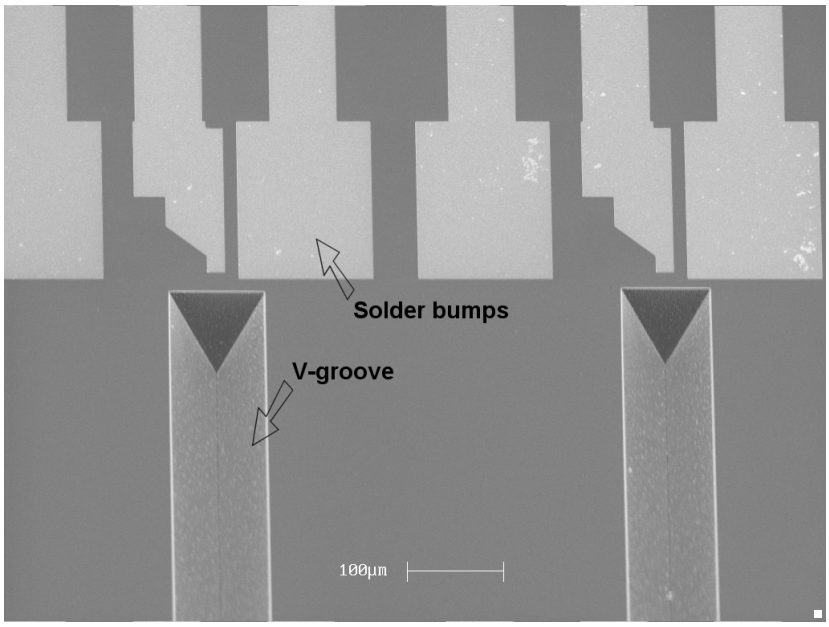


Figure 2.3: Cross section of a wafer going through the fabrication process. A) Growth of thermal oxide and deposition of nitride. The solder pads and the V-grooves are defined by photolithography. B) The pattern is transferred into the nitride layer by RIE. C) Evaporation of Cr and Au. D) Lifting off resist pattern and metal layer in acetone. E) Photolithography process. The pattern covers the solder pads areas. F) Wet etch of metal layer and thermal oxide. Removal of resist layer. G) KOH etch of V-grooves.



(a) An array of laser mounts consisting of V-grooves for the optical fiber and solder pads to connect the laser diode.



(b) Close-up on solder pads and start of the V-groove.

Figure 2.4: SEM picture of silicon motherboard for laser diode packaging.

plane of the silicon wafer. A method for this purpose is suggested in section 7.1.

Actual pigtailing of a laser diode to the silicon motherboard has not been carried out within this project. It was considered to be outside the scope of the project, since no experience with soldering techniques was available at either IONAS A/S nor COM.

2.3 Summary

As an initial introduction to pigtailing techniques a short study of methods used in optoelectronic packaging has been done. In this chapter a short review of different pigtailing methods found in the literature is given.

A new fabrication method based on an existing method has been proposed and fabricated. The advantage of the proposed method is that the vertical alignment between the fiber V-grooves and the solder bumps is not dependent of the alignment accuracy in the photolithography process.

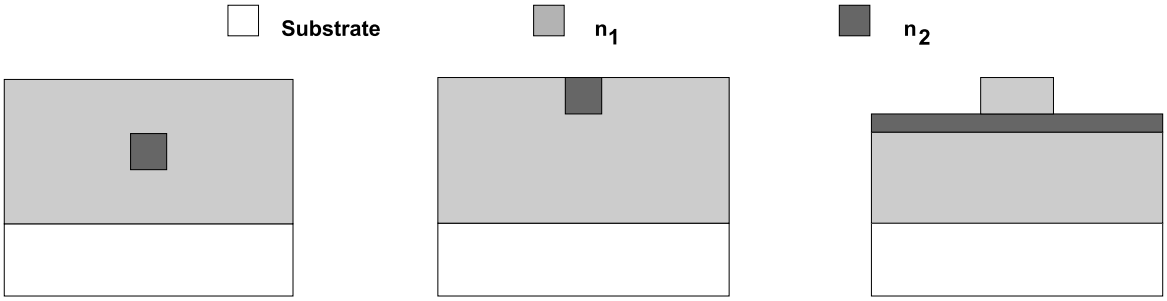
Chapter 3

Planar optical waveguides

An optical waveguide is a light conductor consisting of a slab, strip or cylinder of dielectric material surrounded by another dielectric material of lower refractive index. The light is guided inside the structure by total internal reflection. The guidance of the light can be obtained by several different structures. Most commonly three different types of channel waveguides are used: the buried rectangular waveguide, the embedded strip waveguide, and the strip loaded waveguide. Cross sections of these three different types of planar waveguides are sketched in figure 3.1. In figure 3.1(a) the cross section of a buried rectangular waveguide is shown. For an operational wavelength of 1.55 μm, the buried waveguide can be well matched to the mode of a standard optical fiber and hence obtain a low coupling loss. Due to this, the buried waveguide type is the most common type when considering silica-on-silicon structures. Figure 3.1(b) shows an embedded waveguide structure. This structure is mainly used when fabricating the waveguide by diffusion of dopants into a bulk material. In figure 3.1(c) the cross section of a strip loaded waveguide is shown. The light is confined to the layer in the area below the loading strip.

Most commonly used materials for fabrication of optical waveguides are III-V semiconductors, polymer, or silica. In III-V materials it is possible to integrate active devices (lasers and detectors) as well as passive devices (waveguides, splitters, filters etc.) monolithically. However, the larger propagation and coupling losses make semiconductor waveguides less attractive for applications in fiber optical communication systems. Polymer and silica glass are the two most interesting materials for commercial applications. Polymer waveguide fabrication is an inexpensive technology. However, they have been suffering from problems such as high optical losses and low thermal stability. Recently, results with a low propagation loss at 0.07 dB/cm and good environmental stability have been reported [18]. Silica glass is known from the production of optical fibers to have a very low propagation loss in the telecommunication band as well as a good thermal stability. Both silica and polymer can give a small coupling loss between the waveguide and an optical fiber. In this project the planar waveguides are based on a silica-on-silicon technology.

In the literature various techniques have been explored for the fabrication of silica waveguides. Among the processes for deposition the most frequently used are Flame



(a) Buried rectangular waveguide.

(b) Embedded strip waveguide.

(c) Strip loaded waveguide.

Figure 3.1: Cross sections of three different waveguide structures. n_2 is larger than n_1.

Hydrolysis (FHD), Low Pressure Chemical Vapor Deposition (LPCVD) and Plasma Enhanced Chemical Vapor Deposition (PECVD). To raise the refractive index in the glass film various co-dopants, such as phosphorus, germanium, titanium, and nitrogen, are used.

In the present work glass materials are produced by PECVD. A short introduction to how this deposition technique works is given in section 3.1. Etching of the core structures is done by Reactive Ion Etching (RIE) which is described in section 3.2. The fabrication process in general is described in section 3.3. Finally, in section 3.4 design and measurements on a Variable Optical Attenuator (VOA) are described.

3.1 PECVD deposition

In this work glass materials are produced by Plasma Enhanced Chemical Vapor Deposition (PECVD). The PECVD technique was originally developed for the formation of final passivation layers for integrated electronic circuits.

By plasma-assisted deposition, films are synthesized at low sample temperatures. The plasma is sustained by the introduction of energy from a RF electromagnetic field. The electrons are accelerated by the field, thus gaining energy. The energy is passed to the neutrals through inelastic collisions, hereby producing significant amounts of ions, free radicals, and other excited species without appreciably heating the gas thermally. In this manner, concentrations of free radicals and ions, which would normally be created only at flame temperatures, can be maintained at room temperature. Hence, the plasma deposition largely increases the reactivity of the chemical species at the wafer surface. Without the plasma enhancement a temperature of more than 600 $^\circ$C is required when forming silicon dioxide by pyrolytic deposition [19].

In figure 3.2 the deposition chamber is schematically shown. The chamber is a capacitively-coupled internal electrode reactor working at either 380 kHz or 13.56 MHz. In this work only the low frequency has been used. The chamber consists of two parallel

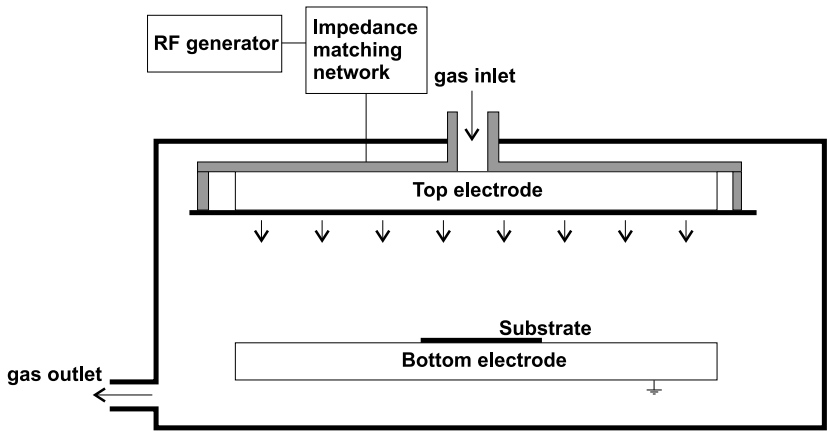


Figure 3.2: Schematic of the PECVD chamber.

aluminum electrodes (top and bottom electrode) of which the top electrode is connected to a RF power generator through an impedance matching network. The silicon wafer is placed on the grounded bottom electrode. The gases are distributed through the top electrode, which is formed as a showerhead. The available gases are: silane (SiH_4), germane (GeH_4), diborane (B_2H_6), phosphine (PH_3), nitrous oxide (N_2O), ammonia (NH_3), and nitrogen (N_2). Germane is used to increase the refractive index of the core layer.

Since the gas chemistry is based on hydrides, such as silane and germane, hydrogen is available in the plasma and may be incorporated in the glass network. The hydrogen is usually bonded within the glass matrix as Si-OH, Si-H, or H_2O. The bonded hydrogen leads to large absorption peaks in the telecommunication bands. The largest resonance occurs at 1506 nm and can be associated with the Si-H bond. Another peak centered at 1400 nm is due to the OH-bond. These absorption peaks in the infrared spectra can be removed by thermal annealing [20, 21].

Another common feature with plasma deposited film is a poor step coverage. Since the deposition rate is proportional to the solid angle of the incoming gas molecules, filling narrow gaps between waveguides is difficult [22]. The deposition rate on the horizontal surfaces is almost three times higher than on the vertical surfaces. When filling a narrow gap, the glass deposited on the upper parts of the side walls will eventually meet, creating so-called keyholes. Adding phosphorus and boron to the top cladding makes it possible to reflow the glass in a subsequent annealing step. However, this method of improving the gap filling is largely constrained by the composition of the top cladding material.

3.2 RIE etching

In this work the core structures of the waveguides are fabricated using Reactive Ion Etching (RIE). One advantage of using a dry etch process rather than a wet chemical etch, is the possibility of obtaining both isotropic and anisotropic structures, without

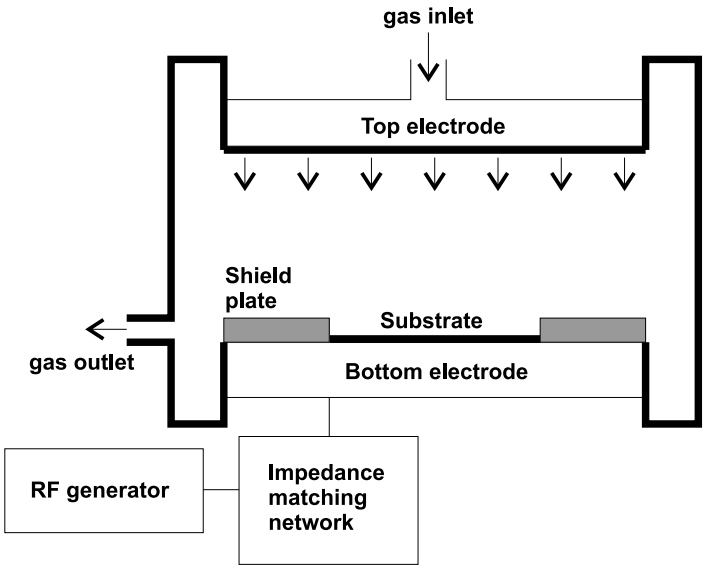


Figure 3.3: Schematic of the RIE chamber.

depending on the crystal orientation of the silicon wafer. Thus giving a large degree of freedom when designing components.

A schematic view of the RIE chamber is shown in figure 3.3. The basic design of the RIE chamber is similar to that of the PECVD chamber. Both chambers have parallel plate electrodes, and the RF power generator and impedance matching network are similar. The major difference between the two chambers is that the RIE bottom electrode is cooled, and that the RF generator is coupled to the bottom electrode. The available gases are CF_4, CHF_3, SF_6, C_2F_6, O_2, N_2, Ar, and H_2. The etching of waveguide cores, done within this project, is described in section 6.1.

3.3 Fabrication method

The waveguides fabricated in this project are buried waveguides, shown in figure 3.1(a). A schematic view of the fabrication process is sketched in figure 3.4. A thermal grown oxide is used as the buffer layer. This is due to the very good optical quality that thermal oxidized silicon exhibit combined with the low production cost. The buffer glass layer has a thickness of 15 μm. The core layer of 6 μm Ge-doped silica glass is deposited on the top of the buffer layer (figure 3.4A). On top of the core layer an etch mask of LPCVD polysilicon is deposited. A photoresist layer is spun onto the polysilicon layer and patterned through a standard photolithography process (figure 3.4B). The pattern is transferred into the etch mask by RIE etching and the photoresist layer is removed. With the polysilicon as mask, the pattern is transferred into the core glass and subsequently the remaining mask material is removed (figure 3.4C). Finally, the waveguide structures are covered with top cladding (figure 3.4D). The top cladding glass is doped with phosphorus and boron and reflown in subsequent annealing steps.

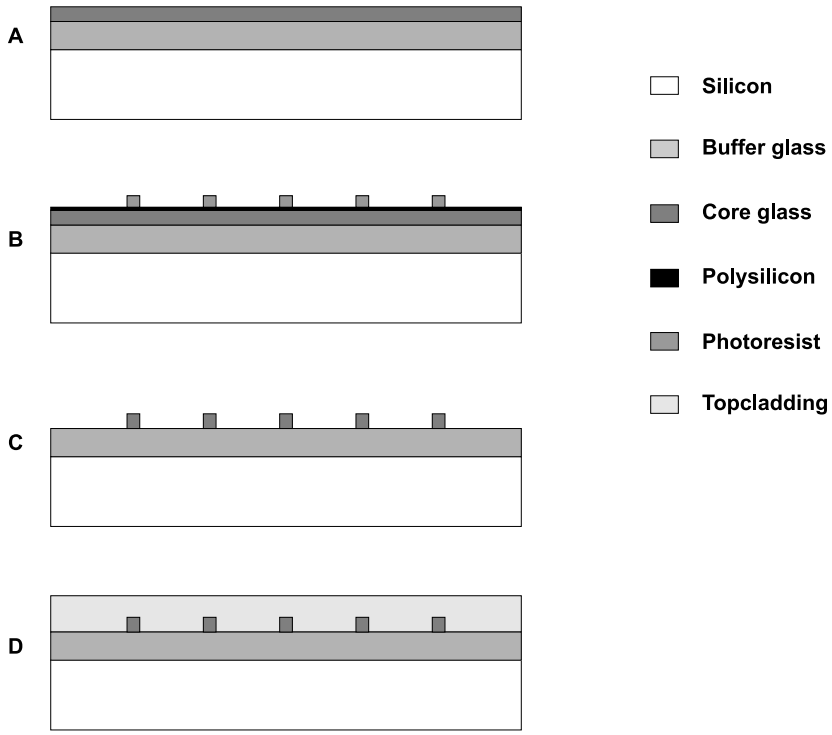


Figure 3.4: The waveguide fabrication process. A) Growing of the buffer and deposition of the core layer. B) Deposition of the polysilicon mask layer and definition of the waveguide pattern by photolithography. C) Pattern transfer into the core layer by RIE. D) Deposition of top cladding and subsequent annealing to reflow the glass.

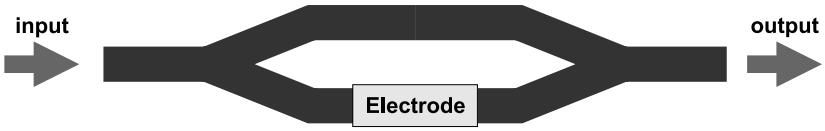


Figure 3.5: Y-splitter based Mach-Zehnder interferometer.

3.4 Variable optical attenuator

A Variable Optical Attenuator (VOA) has been designed and fabricated within this project. The attenuator is designed as a Mach-Zehnder interferometer based on Y-splitters. A schematic view of the Mach-Zehnder interferometer is shown in figure 3.5. The light enters the input arm, is split into two equal signals in the first splitter region and combined again in the second splitter region. On one of the branches a thin metal film heater is placed. Applying a heater current on the electrode makes it possible to shift the phase of the light through the thermo-optical effect [23]. A phase modulator placed in one branch of an interferometer will function as an intensity modulator. If the first Y-splitter divides the optical power equally, the transmitted intensity I_o is related to the incident intensity I_i by

$$I_o = \frac{1}{2}I_i + \frac{1}{2}I_i\cos(\phi) = I_i\cos^2(\frac{\phi}{2}) \tag{3.1}$$

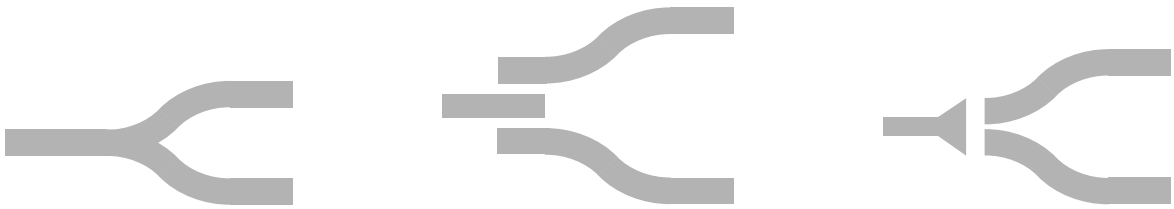
where ϕ is the phase shift difference between the two branches.

A quantitative measure of the VOA performance is the extinction ratio. The extinction ratio is defined as

$$R_{ext} = -10log(\frac{I_{o,max}}{I_{o,min}}) \tag{3.2}$$

where $I_{o,max}$ is the maximum output intensity ($\phi = 0$) and $I_{o,min}$ is the minimum output intensity ($\phi = \pi$). The ratio should be as low as possible to achieve a large attenuation range of the device.

Three different VOA designs have been investigated; the different types are a cosine type VOA, a coupler type VOA and a tapered VOA. The difference between the designs is the layout of the Y-splitter sections. In figure 3.6(a) the traditional Y-splitter design based on cosine bends is shown. The advantage with this splitter design is that the splitting ratio is very insensitive to the wavelength of the light. However, since the distance between the two arms goes down to zero in the splitter region, there can be problems both in resolving the gap in the photolithography process and with keyholes in the top cladding. In figure 3.6(b) the coupler type Y-splitter design is shown. This design has an advantage since it is fairly easy to produce both regarding the photolithography and filling the gaps with top cladding. However, since the splitting ratio of the coupler type Y-splitter is wavelength dependent, the coupler type VOA is expected to work as a narrow band attenuator. In figure 3.6(c) the design of a tapered Y-splitter is shown. The design is a variation of the traditional splitter based on cosine bends, but with a gap between the waveguides in the splitter region. Due to this gap



(a) Cosine type. (b) Coupler type. (c) Tapered type.

Figure 3.6: Schematic view of three Y-splitter designs.

it should be easier to fabricate, both with respect to photolithography and keyholes, than the traditional cosine Y-splitter.

On the fabricated components the refractive index difference between the buffer and the core was chosen to be 0.005, so-called low-delta waveguides. After top cladding deposition the wafer was inspected using an optical microscope. All the VOA's based on the tapered Y-splitter had problems with keyholes in the top cladding. Hence, it is only the VOA's based on cosine bends and coupler's that have been measured. Keyholes in a component depends on the distance between the waveguides, the depth of the etch, the surface tension, the thickness of the deposited glass layer, and the annealing procedure. It is a quite complicated process, which is difficult to predict before fabrication. The splitter design, which was suggested to minimize the keyhole problem, actually was the one having keyholes. This emphasizes the complexity of the top cladding process.

When measuring the components the input and output fibers have to be attached to the component. Otherwise, when applying a heater current, the coupling conditions for the aligned fibers will be corrupted by thermal drift. If the fibers are drifting, it is difficult to get reliable measurements. However, pigtailing of the fibers was not available at IONAS at the time. Therefore, pigtailing of optical fibers and the measurements of the components have been performed by Uniphase. The results are listed in table 3.1. Compared to the device specifications, both the insertion loss and the polarization dependent loss (PDL) of the devices are rather high. Measurements on straight waveguides on the same wafer had insertion losses around 1.5 dB and a po-

Measured Parameter	**Cosine**	**Coupler**	**Specifications**
Insertion Loss in ON state	2.2 dB	2.3 dB	$\leq$ 2.0 dB
Insertion Loss before pigtailing	1.7 dB	2.1 dB	-
Extinction Ration (On/Off)	42.6 dB	39.8 dB	$\geq$ 17 dB
PDL in On state	2.1 dB	2.43 dB	$\leq$ 0.1 dB
PDL in Off state	0.7 dB	0.2 dB	$\leq$ 1 dB

Table 3.1: Measurements on variable optical attenuators (performed by Uniphase).

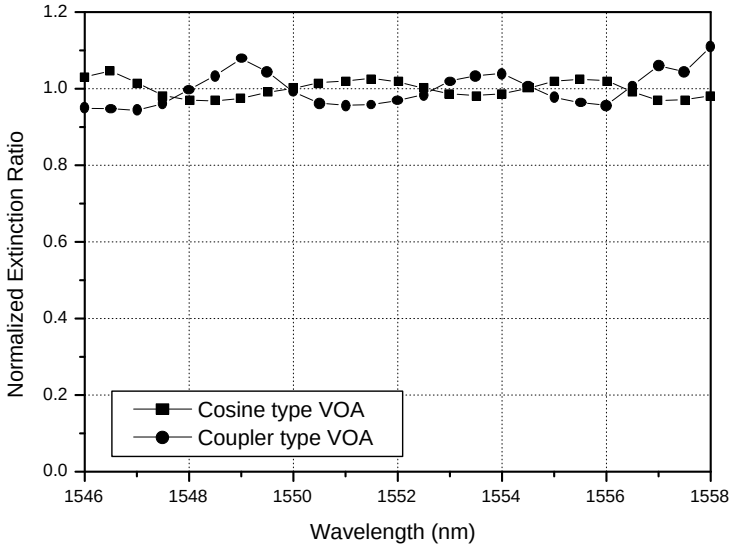


Figure 3.7: Narrow band wavelength dependency of the extinction ratio for the two VOA designs.

larization dependent loss of 1.8 dB. This emphasizes that the problem occurs in the fabrication process and is not due to the design of the VOA's. The used fabrication method is optimized for a larger refractive index difference of 0.01, so-called high-delta waveguides. Apparently, the process optimized for high-delta waveguides is not suited for the fabrication of low-delta waveguides. This will be further discussed in section 6.2. The problem would be solved easily by raising the core refractive index. It remains to be emphasized that the extinction ratio for both measured VOA types was extremely high.

The wavelength dependency of the extinction ratio has been measured for cosine type VOA's and coupler type VOA's. The extinction ratio has been measured in both a narrow band (1546-1558 nm) and a broad band (1500-1580 nm). The results are shown in figure 3.7 to 3.9. To ease the comparison between the two devices the extinction ratio values have been normalized to their mean value of the measured data for the respective device. The wavelength dependency of the extinction ratio has been simulated with a commercial available simulation tool. The simulation results are shown together with the measured data in figure 3.8 and 3.9. The extinction ratio of the measured devices does not depend very much on the wavelength in both the narrow band and broad band regions. The cosine type VOA has a variation of the extinction ratio within $\pm$ 4%. For the coupler type VOA the variation is within $\pm$ 7%. The simulations on the extinction ratio as a function of wavelength show that the coupler type VOA is expected to exhibit a slightly larger wavelength variation than the cosine type VOA. This is in good agreement with the experimental data. In the narrow band measurements figure 3.7 both types of VOA's shows an oscillatory behavior. This

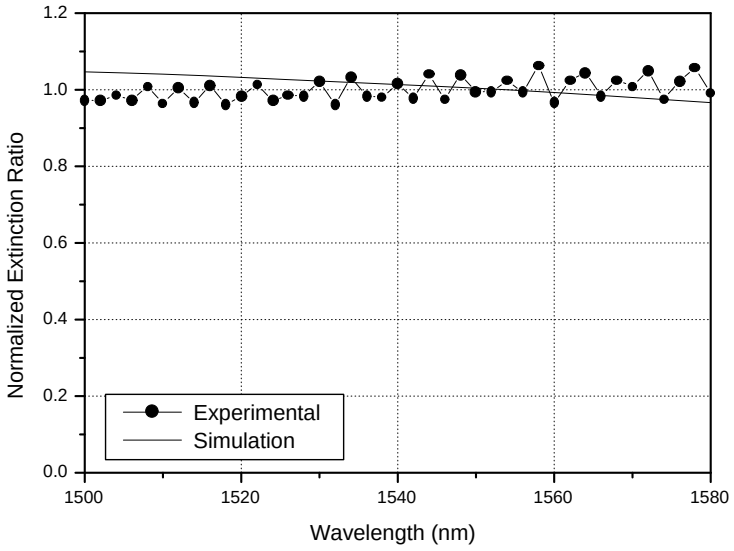


Figure 3.8: Broad band wavelength dependency of the extinction ratio for the cosine type VOA and simulated values.

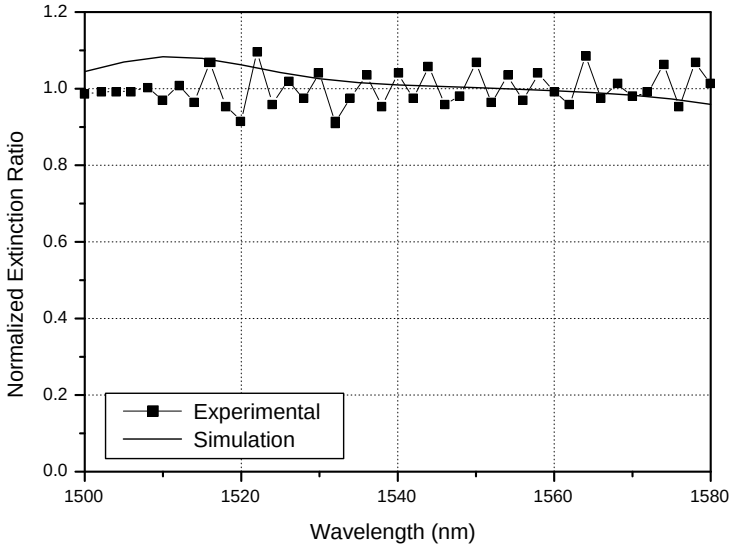


Figure 3.9: Broad band wavelength dependency of the extinction ratio for the coupler type VOA and simulated values.

is not seen in the simulated data. When investigating the measurement data, the same oscillations are seen in the OFF-state measurements. Since the measurements have been carried out by Uniphase, it is difficult to determine, whether it is caused by the measurement setup or is a true wavelength behavior of the devices.

3.5 Summary

The fabrication process of the waveguides is presented step by step in this chapter. The waveguides fabricated are of the buried waveguide type, with the core totally surrounded by a lower refractive index glass.

Variable optical attenuators have been designed and fabricated. The devices showed a very good attenuation range and a low wavelength dependency. However, optimization on lowering the insertion loss and polarization dependent loss still has to be performed.

Chapter 4

Fiber pigtailing of planar waveguides

Integrated optics technology today allows mass production of passive optical chips with low insertion loss. The pigtailing operation remains the most critical step. The fiber to the waveguide connection is the weakest point both in terms of optical characteristics (insertion loss and reflection) and environmental behavior. Pigtailing is also the bottleneck of the whole manufacturing process, because optical fibers have to be attached to all the input and output waveguides. This increases the overall cost of the component.

For commercial applications the pigtailed components have to comply with telecommunication specification schemes. The connection between an optical fiber and a planar waveguide adds coupling and misalignment loss to the waveguide propagation loss. The acceptable loss for such a connection is usually set to the requirements for fiber-to-fiber coupling loss:

$$L \leq 0.2dB/connection \tag{4.1}$$

The interface at the fiber to waveguide connection will also cause a reflection of the signal. Back reflected signals may feed back into the source, a laser emitter, shifting both emission frequency and power. Especially in single-mode optical communication systems, this drastically reduces the system performance [24]. The limit for the back reflection is commonly expressed as a maximum optical return loss, based on the systems requirements. In short range telephony applications or for sensor systems a return loss of -30 dB may be sufficient. While the Bellcore specifications for long range communication systems require a return loss below -50 dB. In Cable television distribution the requirements may reach -55 dB [24].

In section 4.1 equations for coupling loss due to mode mismatch, longitudinal offset, transverse offset, and angular offset between an optical fiber and a waveguide are presented. In section 4.2 these equations are used to calculate the tolerance for the offsets involved in the fiber pigtailing process. Furthermore, the reflection from the fiber to waveguide interface is estimated. Finally, in section 4.3, a short review of fiber attachment methods found in the literature is given.

4.1 Coupling loss

The excess loss for any fiber pigtailed waveguide is the sum of 3 terms: the propagation loss in the structure, the mode-size mismatch between the fiber and the waveguide, and the misalignment between the two core regions. The propagation loss is beyond the scope of this chapter since it depends on the chip fabrication parameters and the waveguide design.

The coupling loss due to the mode-size mismatch and the misalignment may be calculated using the estimation that the field propagating in a weakly guiding single mode planar waveguide may be approximated by an equivalent weakly guiding, step index, circular core optical fiber [25]. Denoting the width of the quadratic core by a the equivalent fiber radius r_ω is given by:

$$r_\omega = \frac{a}{\sqrt{\pi}} \tag{4.2}$$

The equivalence between the fundamental mode of a single-mode fiber and the quadratic core waveguide means that we may use the loss formulas derived by Marcuse for optical fibers [26]. This loss analysis is based on the approximation that the mode in the waveguide may be approximated by Gaussian functions, where the spot size of the mode is given by:

$$\frac{\omega}{r_\omega} = 0.65 + \frac{1.619}{V^{\frac{3}{2}}} + \frac{2.897}{V^6} \tag{4.3}$$

where V is the normalized frequency and is defined by the geometrical and optical properties of the waveguide.

$$V = \frac{2\pi r_\omega \sqrt{n_1^2 - n_2^2}}{\lambda} \tag{4.4}$$

n_1, n_2 are the refractive indices of the core and the cladding, respectively. It is important to note that equation 4.3 is most accurate for V around 2.5 and should otherwise be used with care.

In general the field propagation in the optical fiber and the waveguide will not have the same spot size. The coupling loss due to the difference in the spot size can be calculated by:

$$T = \left(\frac{2\omega_1\omega_2}{\omega_1^2 + \omega_2^2}\right)^2 \tag{4.5}$$

where ω_1 and ω_2 is the field spot size of the waveguide and the optical fiber, respectively. The loss is commonly denoted as the mode mismatch loss.

Misalignment may occur on each degree of freedom. Hence, there are three types of misalignment: longitudinal, transverse, and angular offset. The loss due to the misalignment may be found from the power transmission coefficients [26]. In these equations ω_1 and ω_2 are the field spot size from the fiber and the waveguide, respectively. In figure 4.1 the three types of misalignment are shown and the definitions of the longitudinal offset l_1, transverse offset l_2, and angular offset θ may be seen.

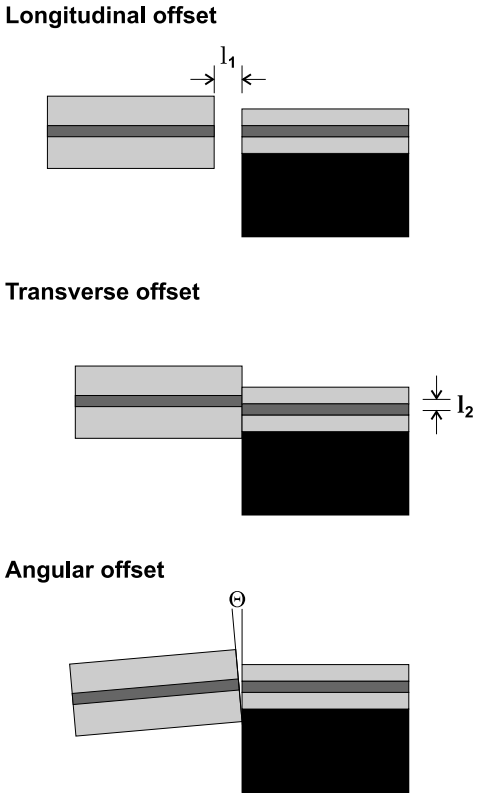


Figure 4.1: Three types of misalignment between fiber and waveguide are longitudinal offset l_1, transverse offset l_2 and angular offset θ.

The coupling loss as a function of the longitudinal offset is given by:

$$T = \frac{4(4Z^2 + (\frac{\omega_1}{\omega_2})^2)}{(4Z^2 + \frac{\omega_1^2+\omega_2^2}{\omega_2^2})^2 + 4Z^2(\frac{\omega_2}{\omega_1})^2} \tag{4.6}$$

where Z is given by: $Z = l_1/(n_2\omega_1\omega_2 k), k = 2\pi/\lambda$

The coupling loss as a function of the transverse offset is given by:

$$T = (\frac{2\omega_1\omega_2}{\omega_1^2 + \omega_2^2})^2 exp[-\frac{2l_2^2}{\omega_1^2 + \omega_2^2}] \tag{4.7}$$

The transverse offset may be in both the horizontal and vertical direction. The total transverse offset l_2 used in Eq. 4.7 is defined as the displacement of the center of the fiber core with respect to the center of the waveguide core.

$$l_2 = \sqrt{\Delta x^2 + \Delta y^2} \tag{4.8}$$

where Δx and Δy are the misalignment in the horizontal and vertical direction, respectively.

The coupling loss as a function of angular offset is given by:

$$T = (\frac{2\omega_1\omega_2}{\omega_1^2 + \omega_2^2})^2 exp[-\frac{2(\pi n_2\omega_1\omega_2\theta)^2}{(\omega_1^2 + \omega_2^2)\lambda^2}] \tag{4.9}$$

4.2 Tolerance of fiber connections

In this project, so-called low-delta waveguides and high-delta waveguides have been fabricated. The two kinds of waveguides only differ in the refractive index of the core glass. The low-delta waveguide has a core refractive index of $n_1 = 1.4500$ at a wavelength of $\lambda = 1500$ nm. The high-delta waveguide has a core refractive index of $n_1 = 1.4540$ at $\lambda = 1500$ nm. The waveguides are squared in shape with a width of $a = 6$ μm. For both types of waveguides the refractive index of the surrounding buffer and top cladding layers are $n_2 = 1.4450$ at $\lambda = 1500$ nm. Entering these parameters into equations 4.2 to 4.4 the equivalent mode field spot sizes of the waveguides are calculated to 5.3 μm for the low-delta waveguides and 3.9 μm for the high-delta waveguides, respectively.

The optical fiber, which has been used throughout this work, has been supplied by Lucent Technologies Denmark. The outer diameter of the fiber is specified to 125.2 μm and the core concentricity to 0.1 μm. The non-circularity of the fiber is 0.1 %. The optical fiber is specified to have a mode field diameter of 9.5 μm at 1310 nm and a cut-off wavelength of 1246 nm. Using the cut-off wavelength the spot size of the standard single-mode fiber is calculated to be 5.45 μm at $\lambda = 1550$ nm.

For a given limit of acceptable coupling loss of L $\leq$ 0.2 dB (equation 4.1) tolerances for the fiber to waveguide misalignment can be calculated from equation 4.5 to 4.9. No significant coupling loss due to mode-mismatch is expected, when pigtailing the low-delta waveguides with a standard fiber, since the two mode field spot sizes are

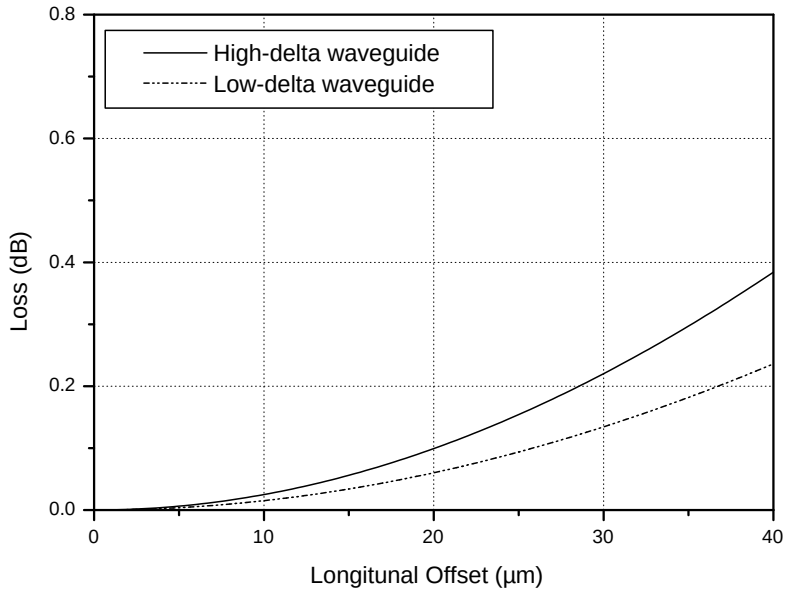


Figure 4.2: Coupling loss (in dB) as a function of longitudinal offset for both low and high delta waveguides.

almost equal. This is not the case for the high-delta waveguides. Using equation 4.5 the mode-mismatch loss from a standard fiber to a high-delta waveguide is calculated to be 0.48 dB per connection.

The coupling loss as a function of longitudinal, transverse, and angular offsets has been calculated for both types of waveguides. This is shown in figure 4.2 to 4.4. The equations 4.7 to 4.9 are all including the mode-mismatch loss. To estimate the tolerance only due to the offset the mode-mismatch loss has been subtracted from the calculated offset loss. It may be seen from the figures that high-delta waveguides are more sensitive to transverse and longitudinal misalignment than the low-delta waveguides. The difference in loss numbers is due to the smaller mode field size of the high-delta waveguide. A loss of 0.2 dB is reached with a longitudinal offset of 28 μm for the high-delta waveguide and 37 μm for the low-delta waveguide. A transverse offset of only 1.0 μm for high-delta and 1.2 μm for low-delta will cause a loss of 0.2 dB. For the angular misalignment the loss reaches 0.2 dB at 0.8 $^\circ$ for the low-delta and 0.9 $^\circ$ for the high-delta. These calculations illustrate that the transverse and angular misalignments are the most critical in the pigtailing process.

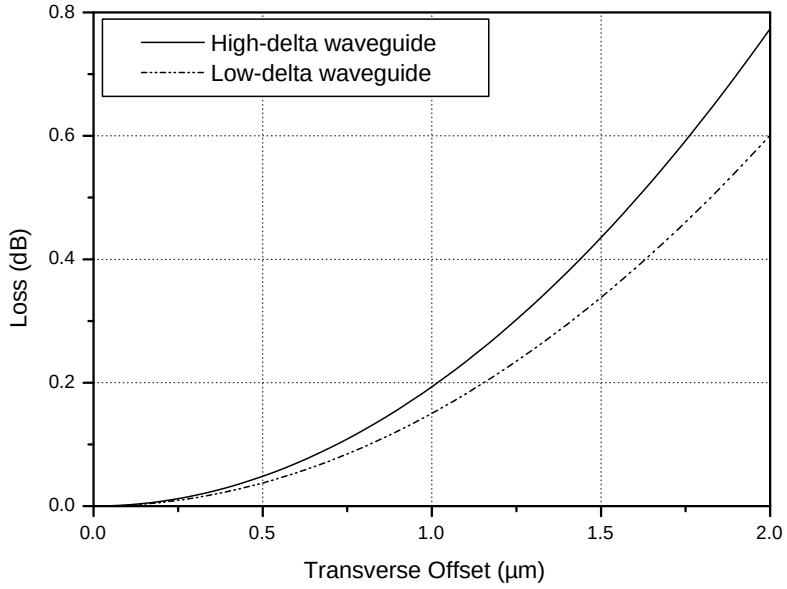


Figure 4.3: Coupling loss (in dB) as a function of transverse offset for both low and high delta waveguides.

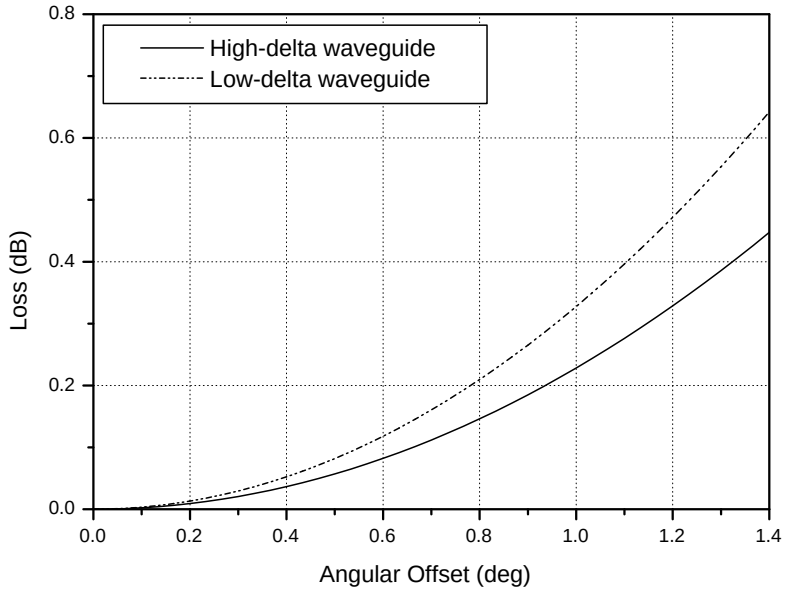


Figure 4.4: Coupling loss (in dB) as a function of angular offset for both low and high delta waveguides.

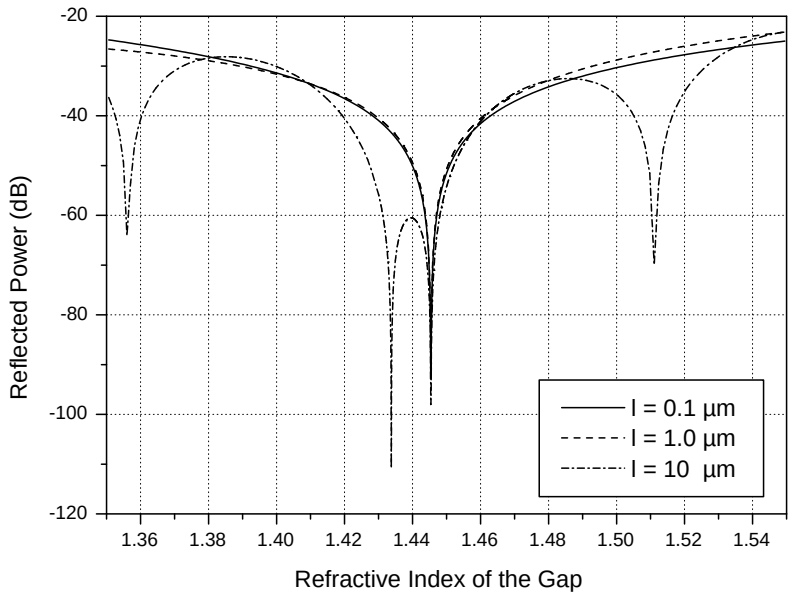


Figure 4.5: Reflected power as a function of the refractive index of the glue n_g, with the length of the gap l as a parameter.

Another aspect that has to be controlled in the pigtailing process is the refractive index of the glue used to attach the optical fibers. If the refractive index of the glue is not matched with the refractive indices of the waveguide and fiber the Fresnel reflection will be high. The Fresnel reflection depends on the index change at both the waveguide and fiber end facets. The reflected light can be written as follows, where the reflectivity R is expressing the reflected power per unit incident power[24]:

$$R = \frac{(\frac{n_f-n_g}{n_f+n_g})^2 + (\frac{n_w-n_g}{n_w+n_g})^2 + 2(\frac{n_f-n_g}{n_f+n_g})(\frac{n_w-n_g}{n_w+n_g})cos(\frac{4\pi n_g l}{\lambda})}{1-(\frac{n_f-n_g}{n_f+n_g})^2(\frac{n_w-n_g}{n_w+n_g})^2 + 2(\frac{n_f-n_g}{n_f+n_g})(\frac{n_w-n_g}{n_w+n_g})cos(\frac{4\pi n_g l}{\lambda})} \tag{4.10}$$

where n_f, n_g, and n_w are the effective refractive indices of the fiber, the gap, and the waveguide, respectively, and l is the length of the gap.

From equation 4.10 the reflected power may be calculated as a function of the refractive index of the glue in the gap. This has been done for different values of the length of the gap as shown in figure 4.5. The effective indices of both the fiber and the waveguide is assumed to be $n_f = n_w = 1.4454$ at $\lambda = 1550$ nm.

The tolerance of the refractive index of the glue in the gap between the fiber and the waveguide may be estimated from figure 4.5. If the length of the gap is 10 μm, a reflection below -30 dB may be obtained for a refractive index of $n_g = 1.4454 \pm 0.045$ whereas a reflection below -55dB is only obtained if $n_g = 1.4454 \pm 0.004$.

Even if the refractive index of the glue is controlled very carefully it is very difficult to obtain a reflection as low as -55 dB as required in cable television distribution.

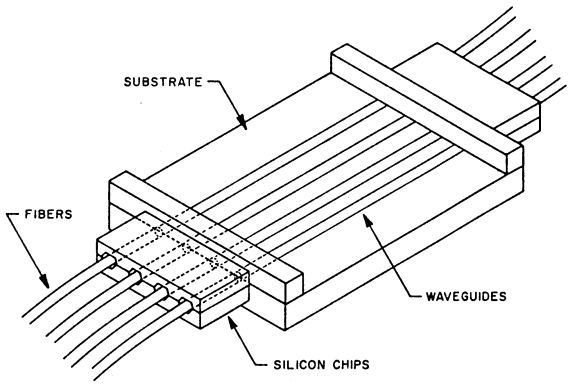


Figure 4.6: Fiber array butt coupled to waveguide substrate for active positioning (from [31]).

Easing the requirements on the refractive index of the glue is done by tilting the facets of the fiber and the waveguide. This reduces the amount of the reflected power that is coupled backwards into the optical fiber. For angled single mode fiber connectors the standard angle is 8°. The light reflected from the interface will have an angle of 16° with respect to the fiber axis. Since this angle is larger than the critical angle for total internal reflection in the fiber most of the light will not be guided backwards by the fiber. It has been shown by Kihara et al. [27] that an 8° tilt of fiber to fiber connection can lower the reflection to -60 dB. It should be noted that tilting the facets does not reduce the total reflection loss at the interface it only lowers the amount of the light that will be guided backwards by the fiber. Tilting the facets of the fiber and the waveguide may be done by polishing.

4.3 Pigtailing methods

Several approaches to fiber attachment of planar waveguide components have been presented in the literature [28, 24, 29, 30]. The main difference between the techniques may be characterized by the alignment of the fiber relative to the waveguide core being done actively or passively. For active alignment light is sent through the component during the pigtailing process and the positioning of the fibers is optimized for maximum light transmission. In passive alignment the fiber is positioned relative to prefabricated structures, without optimization of a light signal through the component.

Attachment of fibers through active positioning has been applied by several groups [31]. The fiber arrays are prepared by gluing single-mode fibers in anisotropically etched silicon V-grooves. After assembly of the fiber array the end facets of the fibers are polished. The waveguide substrate is diced and the end facets are polished to assure a smooth surface. The fiber array and the waveguide substrate is butt coupled, and aligned by simultaneously maximizing the throughput of two of the fiber-waveguide channels (see figure 4.6). Finally, the array is permanently attached using UV-curable glue.

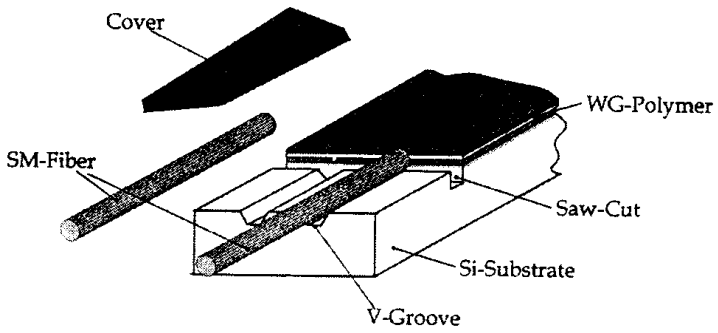


Figure 4.7: A schematic view of a planar waveguide component with a V-groove for passive fiber positioning (from ref. [33]).

Passive pigtailing may be achieved by integrating grooves in the waveguide substrate. The groove may be etched with KOH, which etches with a high selectivity with respect to different crystal planes. This process can be applied for fiber guiding grooves as described by Grant et al. [32, 33]. A component with fiber guiding V-grooves is shown i figure 4.7. The waveguides are processed on the top of the substrate and the V-grooves are subsequently etched at the end of each waveguide. When using KOH-etch the grooves will have walls with an inclination of 54.74 $^\circ$ to all sides. The inclination, where the groove reached the waveguide, is removed by dicing a groove across the component. This dicing process is also used to obtain a smooth end face quality of the waveguide facet. The alignment accuracy achieved through the use of passive alignment is 0.5-1 μm, resulting in a loss penalty of less than 0.2 dB.

One disadvantage of using KOH-etched grooves in the waveguide substrate is that the waveguides have to be oriented with respect to the crystal orientation of the silicon substrate. This gives some restriction on the component design regarding the placement of the grooves. Instead it has been suggested to use dry etched U-grooves as fiber guiding grooves [34, 33, 28]. Another advantage of using a dry etch process is that the width and the depth are independent of each other.

The process suggested by Andersen [28] includes fiber guiding U-grooves which are self-aligned to the waveguide core. The U-grooves are etched into the silicon substrate by RIE. To achieve a good vertical alignment a single mask process is used, i.e. the waveguide mask is used to define both the waveguides and the U-grooves. This way misalignment error due to aligning two lithographic mask levels is avoided. The lowest excess loss due to the misalignment of the fiber is below 0.2 dB/connection.

There are mainly two advantages of the active pigtailing method as compared to the described passive pigtailing methods. Firstly, the fiber attachment does not take up place on the substrate, i.e. there is more space for the waveguides. Secondly, the waveguides can be tested before pigtailing. However, these two advantages may both be implemented into passive pigtailing methods as well. Kihara et al. [35] have proposed a passive pigtailing method for coupling single-mode waveguides to a multifiber array using passive alignment. The device is fabricated by forming alignment V-grooves on

a waveguide chip and precisely molding both end portions of the chip (see figure 4.8). The V-grooves are fabricated by using an accurately controlled mechanical blade based on pre-etched markers. The V-grooves coincide with their designed position with an accuracy better than ± 2.0 μm. The average excess loss is 0.87 dB, mainly due to connection losses.

Another passive alignment technique has been proposed by Massit et al. [30]. The design is based on a silicon microbench on top of which the required functions are flip-chip hybridized (see figure 4.9). One key point is that the optical axis height of the different components is adjusted by simply controlling the solder cylinder radius before solder reflow. The positioning in the horizontal direction is determined by the positioning of the solder pads. This method has been used to align a Fabry-Perot laser diode to a 1-2 splitter. Misalignment in the horizontal direction has been measured to below 0.5 μm. In the vertical direction the alignment is better than 1 μm, and the longitudinal displacement is approximately 10 μm.

4.4 Summary

In this chapter the loss resulting from the coupling between an optical fiber and a planar waveguide is estimated. The loss is estimated as a function of the offsets between the two core regions. To obtain a connection loss below 0.2 dB the longitudinal, transverse and angular offset should be below 28 μm, 1.0μm, 0.9 $^\circ$ for the high-delta waveguides and better than 37 μm, 1.2 μm, 0.8 $^\circ$ for the low-delta waveguides.

The reflected power as a function of the refractive index of the glue in the gap between the fiber and the waveguide has been estimated. To obtain a low Fresnel reflection the refractive index of the glue has to be matched with the refractive indices of the waveguide and the optical fiber. A reflection below -30 dB may be obtained for a refractive index of $n_g = 1.4454 \pm 0.045$, where as a reflection below -55 dB is only obtained if $n_g = 1.4454 \pm 0.004$.

Fiber pigtailing methods can be divided into two groups using either passive or active alignment techniques. A short description of fiber pigtailing processes found in the literature is given.

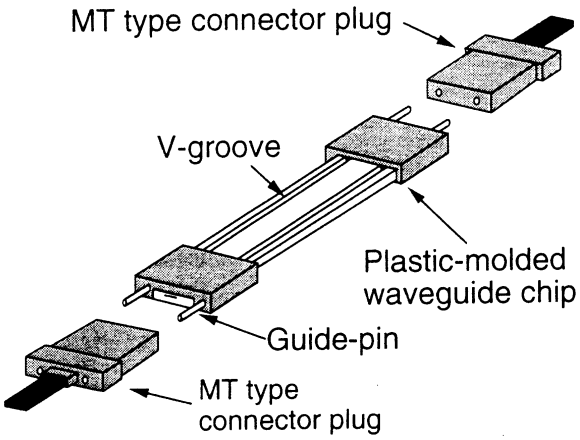


Figure 4.8: Structure of optical device for coupling single-mode planar waveguide to a multifiber array (from ref. [35]).

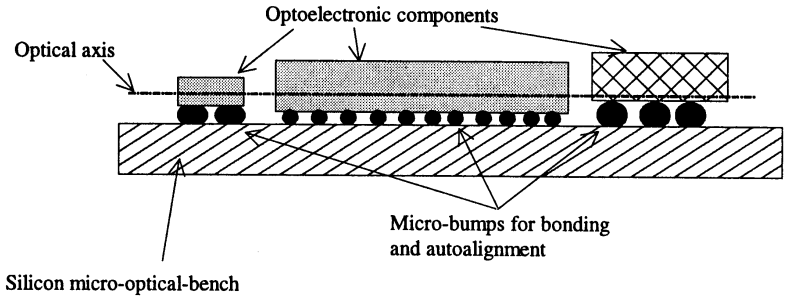


Figure 4.9: Schematic view of the microbench concept (from ref. [30]).

Chapter 5

A new passive pigtailing method

A method for connecting an optical fiber to a planar optical waveguide is developed in which the end facet of a waveguide chip is abutted against the end facet of an array of optical fibers. The assembly is completed with a third piece (top plate) containing micro machined alignment rails, which fits into alignment trenches on both the waveguide chip and the fiber array.

In section 5.1 the principle behind the pigtailing method developed in this project is further described. Before designing the masks, initial processing investigations have been made. Section 5.2 describes the result of these experiments and the waveguide mask layout. The fabrication scheme and the mask designs of the fiber array carrier are described in section 5.3. Finally, in section 5.4 the fabrication scheme and mask designs of the top plate are described.

5.1 A new passive pigtailing method

A new fabrication process has been developed for components, which can be fiber connected by passive fiber attachment. The method involves three different major parts: a waveguide chip with alignment trenches, a fiber array carrier with KOH etched V-grooves for optical fibers and alignment trenches, and finally a top plate with alignment rails that aligns the two other substrates with respect to each other. A schematic view of the three substrates is shown in figure 5.1.

In figure 5.2 a schematic view of the cross sections in the alignment areas is shown. Both the fiber array and the top plate are etched by KOH. Therefore, the crystallographic plane of the silicon wafer defines the angles of the alignment rail and the alignment trench. Hence, they fit perfectly together (figure 5.2(a)). On the waveguide chip (figure 5.2(b)) the alignment rail hits the two upper edges of the alignment trench when correctly aligned.

The waveguide chip is fabricated with a PECVD process. To lower the cost of the extra processing for fabrication of the alignment trenches long expensive processes have been avoided. Hence, wherever possible, batch processes have been chosen. In particular etching through the top cladding would be expensive if done by RIE etch. To avoid this the fabrication process is developed so a wet-etch process can be used.

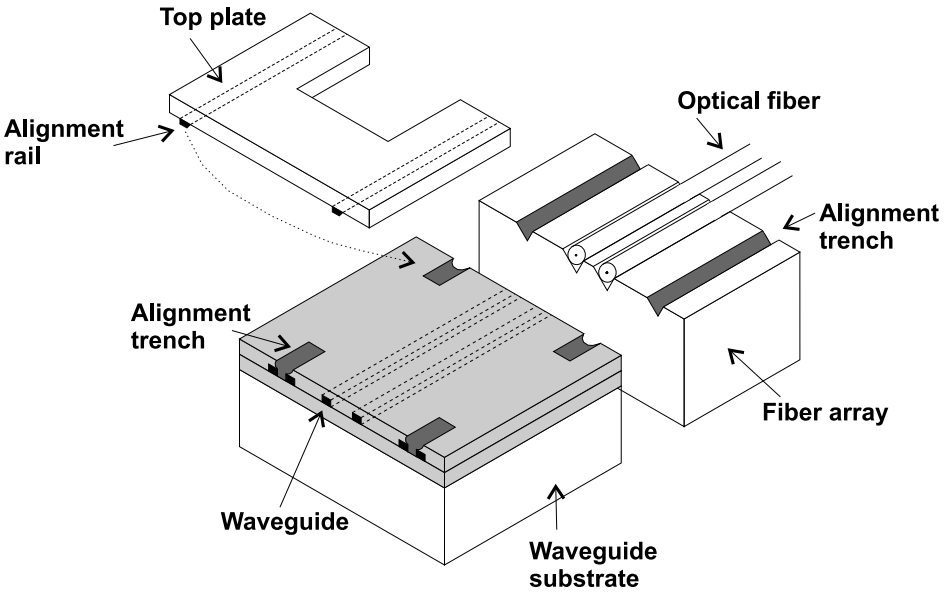
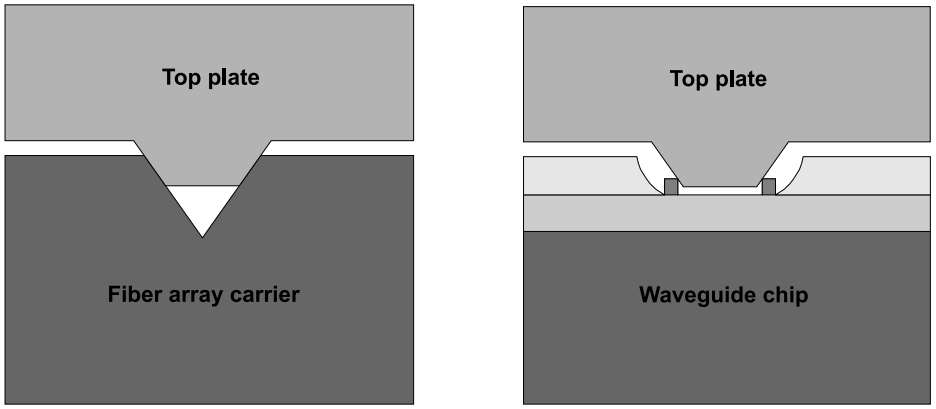


Figure 5.1: Schematic of a passive connection method using a top plate with alignment rails to align the fiber array to the waveguide chip.



(a) The fiber array carrier aligned by means of a top plate alignment rail.

(b) The waveguide alignment trench aligned by means of a top plate alignment rail.

Figure 5.2: Details of the alignment structures.

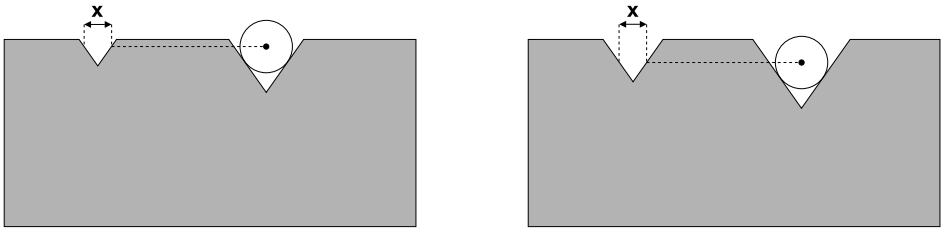


Figure 5.3: A systematic error in the line widths makes the alignment position and the fiber core shift together vertically.

One important factor in the waveguide chip fabrication is that the alignment trenches are defined in the same mask level as the waveguides. This way the alignment accuracy in the horizontal direction is determined by the mask writing process rather than mask re-alignment accuracy in subsequent photolithography steps. The registration of the mask is specified to 0.15 μm by the mask supplier. The alignment trench is made within the core glass layer providing the point of reference for the vertical alignment. An offset in the width of the alignment trench would cause a vertical misalignment. This is discussed further in section 5.2.

Wet etching with a mixture of potassium hydroxide and water (KOH) is used to fabricate both the fiber array carrier and the top plate. To assure a good control of the width of the grooves it is important that the mask is aligned to the {110} crystal plane of the silicon substrate. This is obtained by etching test structures into the wafer revealing the {110} plane and is described in details in section 7.1. When fabricating the fiber array carrier the V-grooves for the optical fibers and the alignment trenches are defined and etched in the same process steps. Hereby, the horizontal alignment is given by the mask specifications. The widths of the V-grooves and the trenches are calculated so the center of the fiber core corresponds to a specific width of the alignment trench. The width and position of the alignment trench and the fiber core do not depend on systematic variations of the line widths at the wafer surface. This is due to the fact that the fiber core and the alignment position move together vertically, remaining their relative alignment. This is shown schematically in figure 5.3. The absolute width of the structures is not critical as long as the line width of the V-grooves and the line width of the alignment trench differs from the line widths on the mask with the same value. This makes the alignment method very tolerant to typical fabrication errors such as wrong exposure time in the photolithography step.

The fabrication process of the top plate is similar to the fabrication process of the fiber array carrier. The alignment rail fits into both the waveguide chip and the fiber array carrier providing the horizontal alignment between the two parts. Like on the fiber array carrier, the alignment position of the two rails moves together vertically. This makes the vertical alignment of the top plate independent of systematic offsets of the line width. If the alignment rail is to small it could reach the bottom of the alignment trench instead of stopping at the upper edge of the alignment trench. Furthermore, the height of the alignment rail has to be large enough to prevent the top plate to stop at the upper surface of neither the waveguide chip nor the fiber array

carrier.

There are three main advantages with this pigtailing process. First, the mask writing process provides the horizontal alignment for all the three parts. This means that the alignment accuracy does not depend on the re-alignment accuracy in the aligner. Second, the vertical alignment accuracy of the top plate and the fiber array carrier is insensitive to systematic offsets of the line width. Third, it is possible to test the performance of the waveguide chip before pigtailing.

An offset of the widths of the structures in the pigtailing method will cause a misalignment between the fiber core and the waveguide core. Offsets on all three parts will contribute to the misalignment. Since the parts are fabricated on separate substrates the offsets may be considered to be independent and distributed as a normal distribution. The total standard deviation σ_{total} can be found by adding the individual standard deviations:

$$\sigma_{total} = ({\sigma_v}^2 + {\sigma_{va}}^2 + {\sigma_{ta}}^2 + {\sigma_{wg}}^2)^{\frac{1}{2}} \tag{5.1}$$

where σ_v is the standard deviation of the V-groove width, σ_{va} is the standard deviation of the width of the fiber array alignment trench, σ_{ta} is the standard deviation of the width of the top plate alignment trench, and σ_{wg} is the standard deviation of the width of the waveguide alignment trench.

An offset in the widths of the structures will cause a misalignment in the vertical direction due to the anisotropic behavior of the KOH etch. The relation between an offset in the line width and the vertical misalignment is given in appendix B, equation B.4. Furthermore, the core concentricity of the optical fiber will contribute to the total misalignment. The standard deviation of the misalignment of the total pigtailing process can be expressed by:

$$\sigma = ((2\tan(\theta)\sigma_{total})^2 + \sigma_f^2)^{\frac{1}{2}} \tag{5.2}$$

where θ is defined by crystallographic considerations to 35.26°, and σ_f is the core concentricity of the optical fiber. For the optical fiber, which has been used in this work, the core concentricity is specified to 0.1 μm.

Variations in the diameter of the optical fiber, misalignment of the optical fiber in the V-groove, or offsets in the positioning of the alignment structures will furthermore contribute to the total misalignment between the optical fiber and the waveguide core. These misalignments can only be estimated indirectly based on the connection loss.

5.2 Waveguide chip

The fabrication of the waveguide substrate is shown step by step in figure 5.4. The waveguides are fabricated as explained in Chapter 3 and shown in figure 3.4. After the buffer and core layers are fabricated the waveguide core region and the alignment trenches are defined in a first photolithography step. The pattern is transferred to the core layer by a RIE glass etch (figure 3.4A). The height of the waveguide cores and the alignment trenches is 6 μm. A layer of polysilicon is deposited on the wafer and

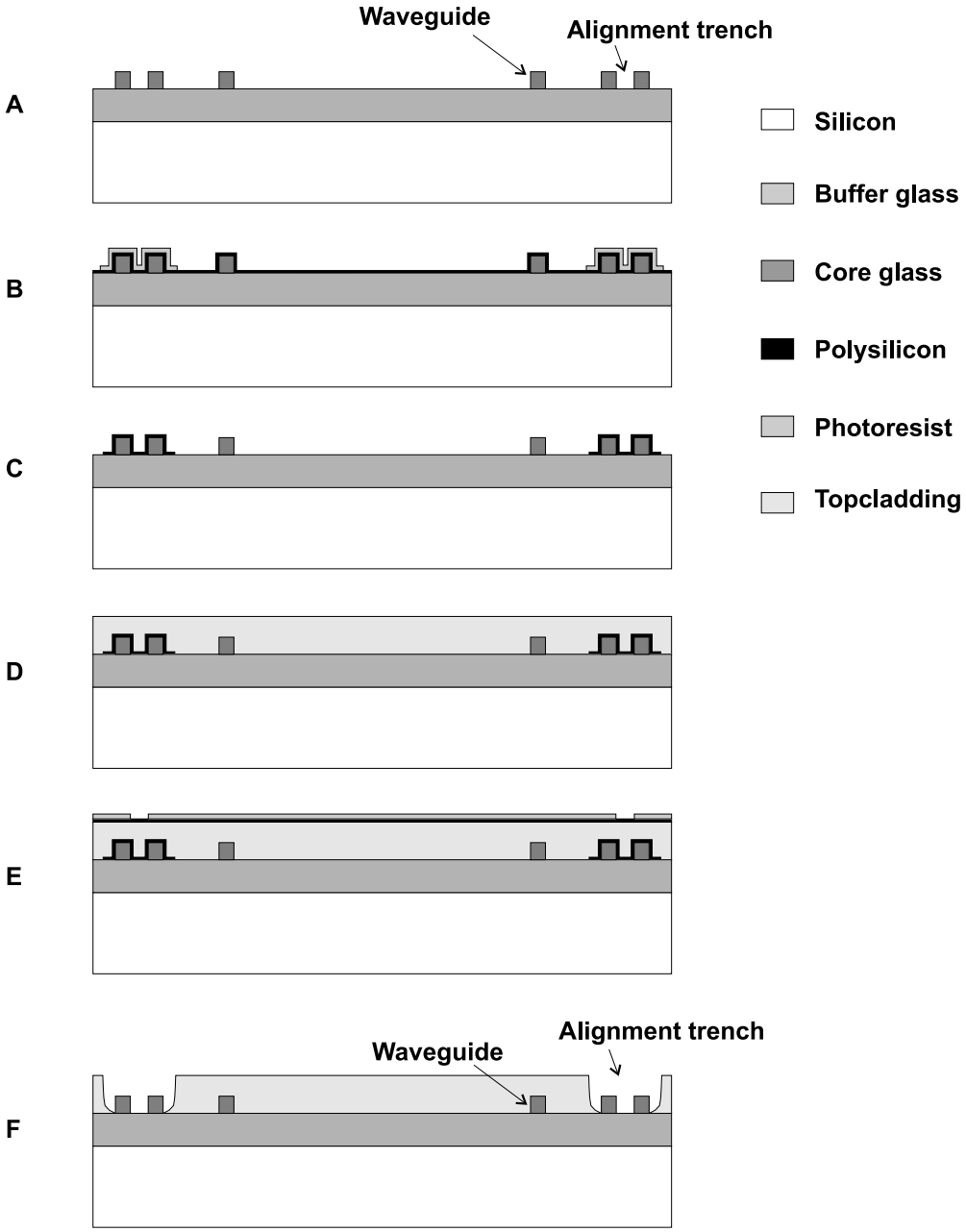


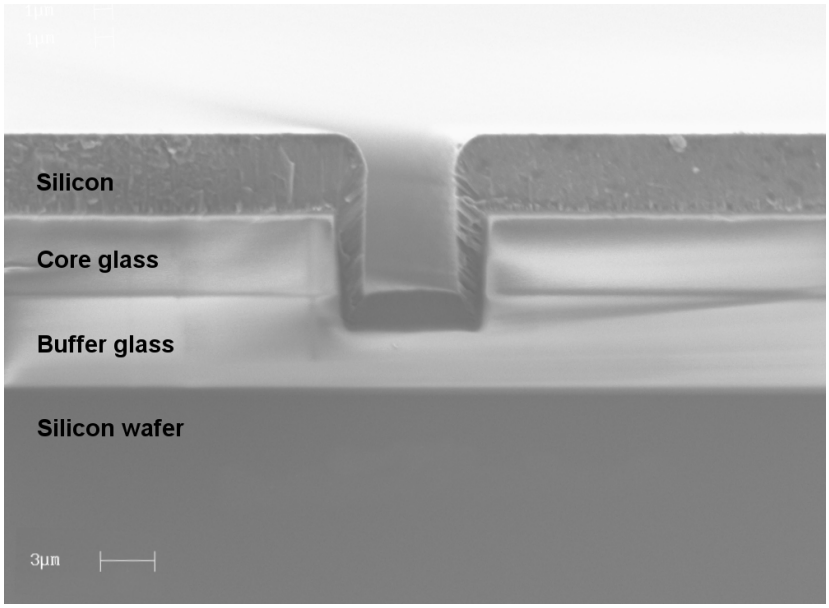
Figure 5.4: Process steps for fabrication the waveguide chip. A) Growth of buffer layer and deposition of core layer. The waveguides and alignment trenches are etched by RIE. B)Deposition of an etch stop layer of polysilicon. Photolithography defines the pattern. C)The resist pattern is transferred into the polysilicon layer by RIE. D) Deposition of top cladding. E) Deposition of an etch mask of polysilicon. Pattern to define the etch is fabricated by photolithography and RIE. F) Wet etch is used to uncover the alignment trenches.

patterned with caps covering the alignment trenches only (figure 3.4B). The polysilicon in the waveguide region is subsequently removed by an isotropic RIE etch (figure 3.4C). The remaining polysilicon caps are required as an etch stop in a later process step. Subsequently, the whole wafer is covered with top cladding (figure 3.4D). Polysilicon is deposited on the top cladding and patterned with the third lateral patterning step. The final patterning step serves to open a window in the top cladding at the location of the alignment trenches. The polysilicon above the alignment trenches is removed by RIE etch (figure 3.4E) and the top cladding is etched isotropic down to the polysilicon stop layer using buffered hydrofluoric acid (BHF). Finally, the polysilicon in the trenches and on top of the wafer is removed in a short KOH etch (figure 3.4F). A detailed process sequence is listed in appendix C.

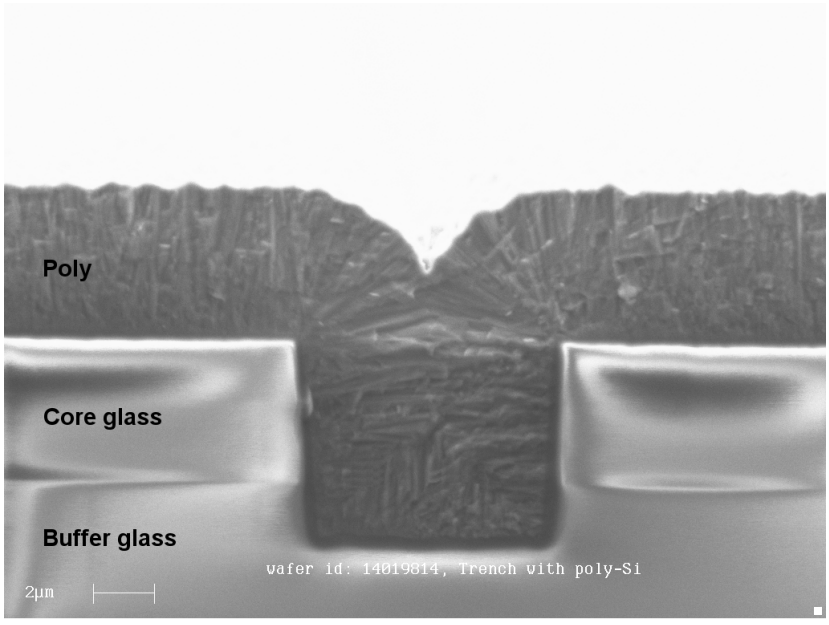
The alignment accuracy of the second and third mask is not critical. A re-alignment accuracy of approximately 5-10 μm is sufficient for the two photolithography steps.

Before making the mask designs some initial experiments were carried out to investigate which kind of etch stop layer could be used above the alignment trenches. A standard waveguide mask was used with a negative photolithography process (to obtain trenches in the glass instead of waveguides). The trenches were etched in the core glass with a standard RIE glass etch. On a first wafer there was sputtered 5 μm of amorphous silicon. On a second wafer 5 μm of LPCVD polysilicon was deposited. In figure 5.5(a) a SEM picture of the cross section of the trench filled with sputtered amorphous silicon is shown. In figure 5.5(b) the corresponding SEM picture is shown, where the trench is filled with LPCVD polysilicon. The sputtered amorphous silicon does not have a good step coverage. A thick layer of material would have to be used to obtain a sufficiently protective etch stop layer. The polysilicon however has good step coverage and the whole trench is filled with polysilicon. Therefore polysilicon is used as BHF etch stop layer.

In another experiment the BHF etch process was investigated. The fabrication process for this experiment is shown schematically in figure 5.6. The same waveguide mask is used in all three mask layers: First for processing of the trench in the core layer (negative photolithography process), second for removal of the polysilicon between the alignment trenches, and finally, after top cladding and a polysilicon deposition on the top, to open the mask for the BHF etch. The result of this experiment is shown in figure 5.7. Both the second and the third mask are misaligned to the left. Since the width of the second mask is the same as the first mask, BHF reaches the sides of the alignment trench and starts etching the buffer layer. It can be seen that the polysilicon was not removed by BHF and may therefore be used as an etch stop layer. To ensure that the BHF do not start etching the core and buffer layer the width of the polysilicon etch stop layer has to be larger than the width of the alignment trench itself.



(a) Filled with 5 μm sputtered amorphous silicon.



(b) Filled with 5 μm LPCVD polysilicon.

Figure 5.5: SEM pictures of a trench filled with silicon.

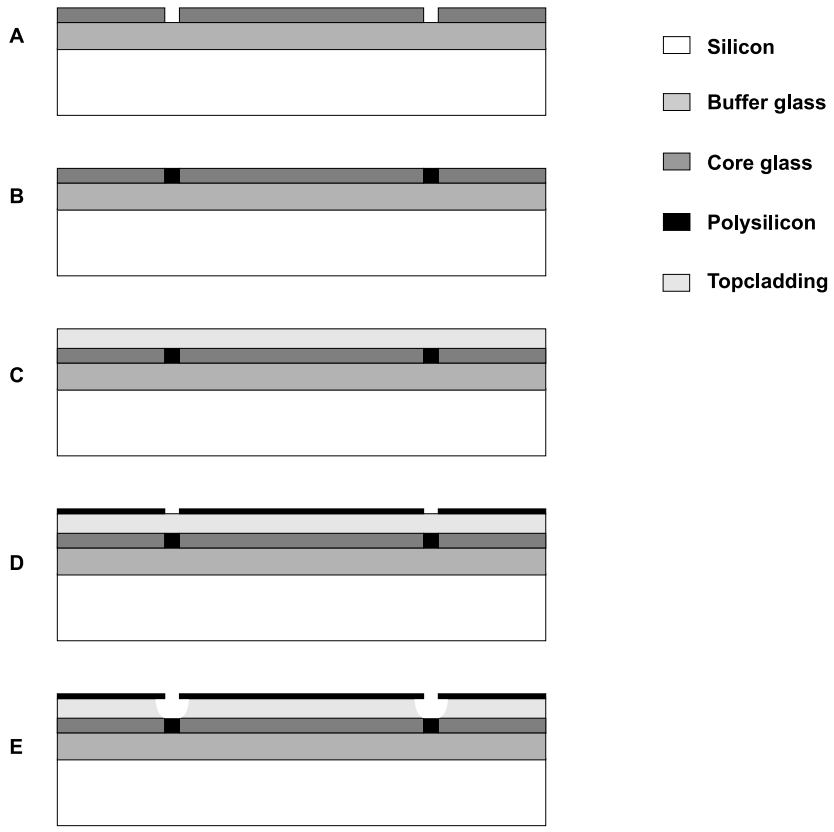


Figure 5.6: Process steps for the BFH etch test. A) Growth of buffer layer and deposition of core layer. Negative photolithography and RIE defines trenches in the core layer. B) Deposition of an etch stop layer of polysilicon. The polysilicon layer between the trenches is removed by RIE. C) Deposition of top cladding. D) Deposition of an etch mask of polysilicon. A pattern to define the etch is fabricated by photolithography and RIE. E) Wet etch is used to reveal the trenches.

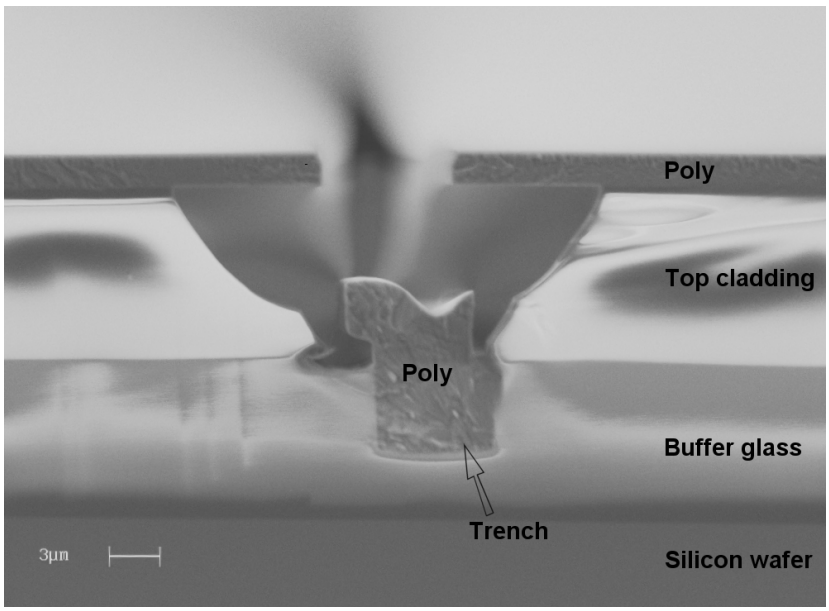


Figure 5.7: BHF etch test with three photolithography steps.

To avoid the alignment problem a similar experiment was performed without removing the polysilicon in the areas between the trenches. The cross section may be seen in figure 5.8. Both the top cladding glass and the glass below the polysilicon are etched by the BHF. This is caused by holes in the etch stop layer. Stress in the thick polysilicon layer would cause a crack at the corners of the trench. It should be noted that the etch rate of the un-doped buffer glass (and also the core glass) is approximately three times larger than of the phosphorus and boron doped top cladding. Hence, it is important to avoid the BHF to reach these glass layers. It can be concluded, that 5 μm of polysilicon is too thick to be used as an etch stop layer.

Finally, an experiment with a 1 μm thick polysilicon etch stop layer was performed. In this experiment the polysilicon did not break due to stress and worked as a stop layer for the BHF etch. This is shown in figure 5.9.

Two conclusions can be drawn from these experiments. First, a 1 μm polysilicon layer will work as a sufficient etch stop protection. Second, the width of the caps on the second mask has to be wider than the alignment trench to prevent the BHF to reach the core and buffer layers.

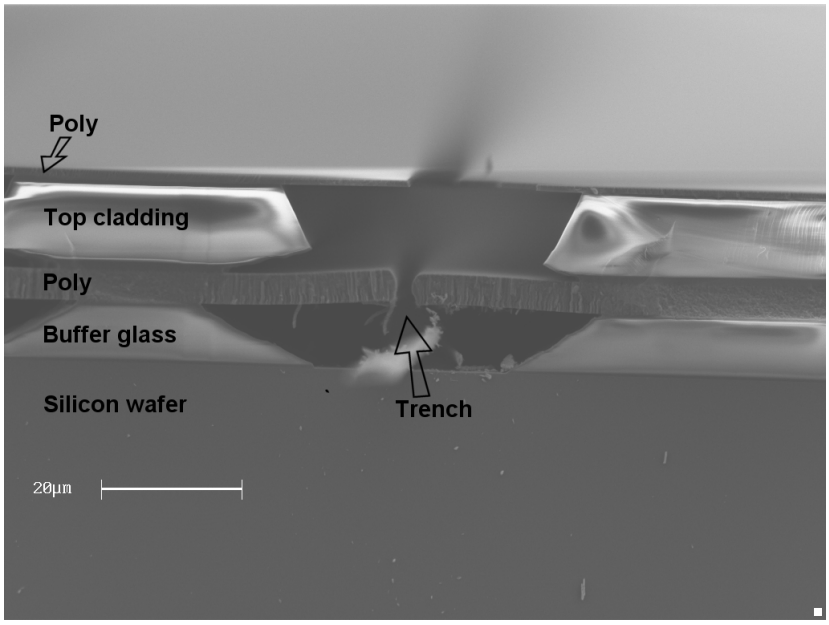


Figure 5.8: BHF etch test with a 5 μm polysilicon layer.

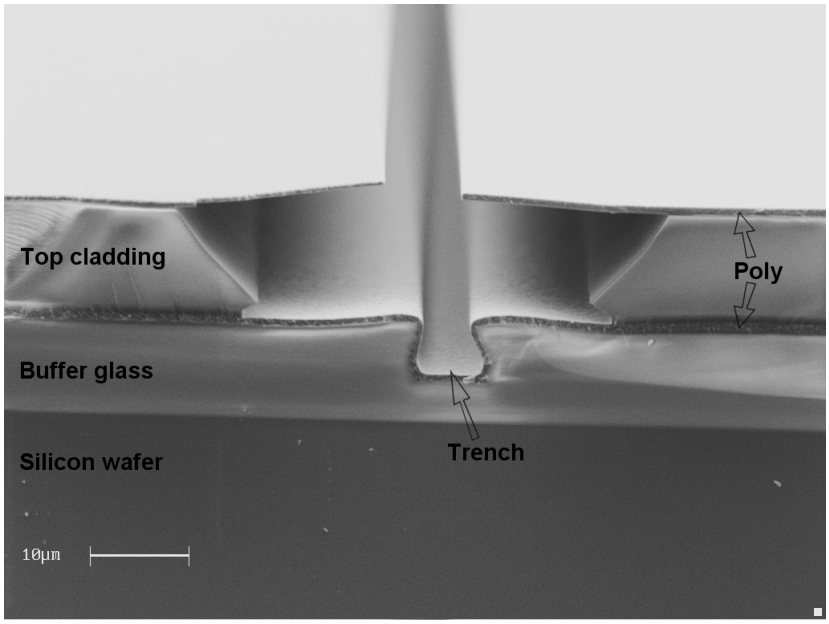


Figure 5.9: BHF etch test with a 1 μm polysilicon layer.

5.2.1 Mask layout

The designed waveguide mask consists of 16 chips with identical waveguide layout, but different layout of the alignment trenches. A schematic view of the waveguide chip may be seen in figure 5.10. Each waveguide chip consists of two straight waveguides, four bends, a splitter and a coupler. All waveguides are 8 μm wide with bend radii larger than 5 mm.

Three different widths of the waveguide trench have been chosen to 15, 30 and 60 μm, respectively. Five chips are made with each of the three widths. It is important to achieve the correct width of the alignment trenches. If the width differs from the design it will affect the vertical alignment accuracy. During the RIE glass etch a reduction of the line width of the structures will take place. The absolute line width reduction depends on the mask layout. For the same mask the line width reduction has a standard deviation of approximately 0.05 μm [36]. To allow for an uncertainty of the RIE etch the line width reduction is varied from 0.25 μm to 1.25 μm in steps of 0.25 μm. Hence, the standard deviation of the width of the waveguide alignment trench is $\sigma_{wg} = 0.05$ μm, and the maximum deviation is $\sigma_{wg,max} = 0.25$ μm. A 0.25 μm offset of the width of the alignment trench correspond to a vertical misalignment of 0.18 μm (see appendix B).

On the second mask for defining the polysilicon caps above the alignment trenches, the pattern is made 50 μm wider than the corresponding alignment trench (both parallel and orthogonal to the waveguides). This is done to ensure that the BHF do not reach the core and buffer glass. On the third mask, for opening up the polysilicon layer for the BHF etch, the width of the pattern has the same size as the width of the alignment trenches on the waveguide mask.

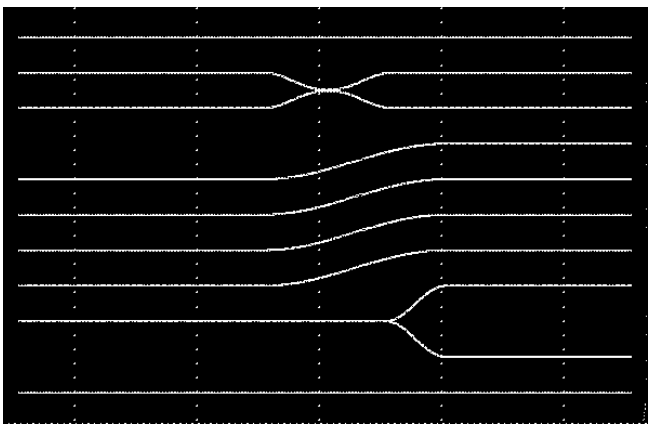


Figure 5.10: Schematic view of the waveguide chip layout.

5.3 Fiber array carrier

The fiber array carrier consist of 11 V-grooves for the optical fibers and two alignment trenches. A cross section is shown schematically in figure 5.11 (only with two V-grooves though). Both the V-grooves for the fibers and the alignment trenches are etched with KOH in the same process step. The fiber V-grooves are designed so the middle of the fiber core is placed 18.3 μm below the surface of the silicon wafer. The width of the alignment trench is determined so it equals the width of the alignment rail 15 μm below the surface of the silicon wafer. Calculations of the width of the V-grooves and the alignment trenches can be seen in appendix B. As described previously in this chapter the vertical alignment accuracy is insensitive to systematic offsets of the line width. However, if the offset only appears in one of the structures this would affect the alignment accuracy. For example, a line width error of 0.5 μm of a V-groove would cause a 0.35 μm shift of the center of the fiber core.

The fabrication process of the fiber array is shown schematically in figure 5.12. First, an alignment pattern is etched into the silicon wafer to reveal the crystal orientation. This step is not shown in figure 5.12, but discussed further in chapter 7. A nitride layer is used as an etch mask for the KOH etch. The nitride layer is deposited using a LPCVD process. Both the alignment trenches and the fiber V-grooves are defined in the same photolithography step (fig. 5.12A) The mask is transferred into the nitride layer using either RIE or wet etch (fig. 5.12B). The choice of the nitride etch process is discussed in section 7.3. The pattern are etched in to silicon layer using a standard KOH etch and the nitride layer is subsequently removed (fig. 5.12C). A detailed process sequence is listed in appendix C.

On the mask layout of the fiber array carrier five different chips are made for each of the corresponding widths of the waveguide alignment trench. Even though a systematic offset on the line width is supposed to be insignificant the values of the widths have been varied with -0.6 μm to +0.6 μm in steps of 0.3 μm.

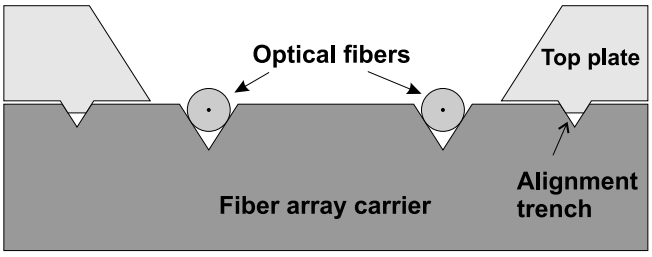


Figure 5.11: Schematic of a cross section through the fiber array.

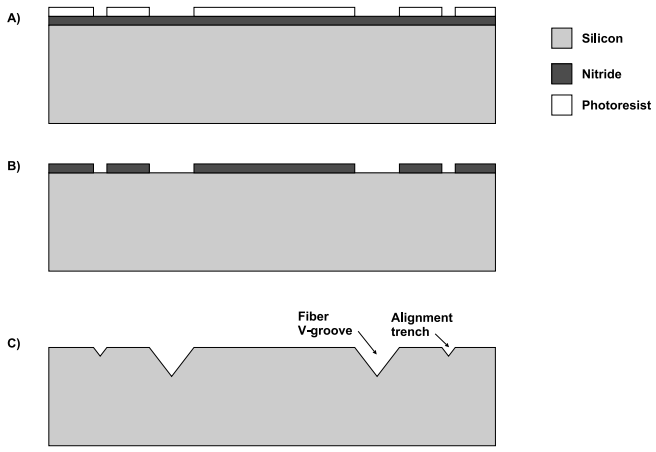


Figure 5.12: Process step for fabrication of the fiber array carrier. A) Nitride is deposited on the silicon substrate and the alignment trenches and fiber V-grooves are defined in a photoresist pattern. B) The structures are etched into the nitride layer. C) The structures are etched in KOH and the nitride layer removed.

5.4 Top plate

The top plate consist of two alignment rails and a recess. A schematic view of the top plate is shown in figure 5.13. The recess is necessary since the optical fibers sticks out above the surface of the fiber array carrier. Etching through the wafer from the backside opens the recess. Calculations of the width of the alignment rails and the backside pattern are described in appendix B. If the line width of the alignment rail is too small, the rail will touch the bottom of the waveguide alignment trench instead of being aligned by the edges of the trench. This would happen if the alignment rail were 1.3 μm smaller than the design value.

The fabrication process of the top plate is shown schematically in figure 5.14. First the crystal orientation of the silicon wafer is determined (not shown in the figure, see chapter 7). LPCVD nitride is deposited on the wafer to be used as an etch mask in KOH. After the nitride deposition the alignment rails are defined in a standard photolithography step. The mask is transferred to the nitride layer (fig. 5.14A). The pattern is etched into the silicon wafer using KOH and the nitride is subsequently removed (fig. 5.14B). A mask layer of nitride is deposited for the backside KOH etch is deposited. The layer is also protecting the front side of the substrate during the etch. The backside pattern is defined in a photolithography step and the mask is transferred to the nitride layer (fig. 5.14C). Etching through the wafer from the backside is done with KOH. Finally the nitride layer is removed (fig 5.14D). A detailed process sequence is listed in appendix C.

In the mask layout the same variations of the line widths is incorporated as on the fiber array carrier.

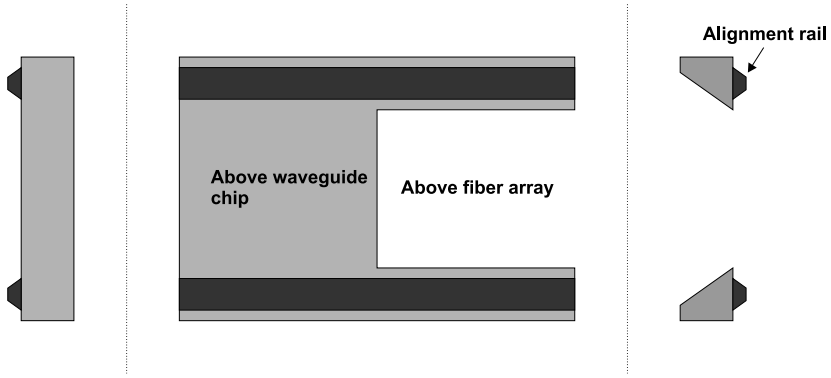


Figure 5.13: Schematic view of the top plate. Above the fiber array between the alignment rails is etched through the wafer to ensure place to for the fibers.

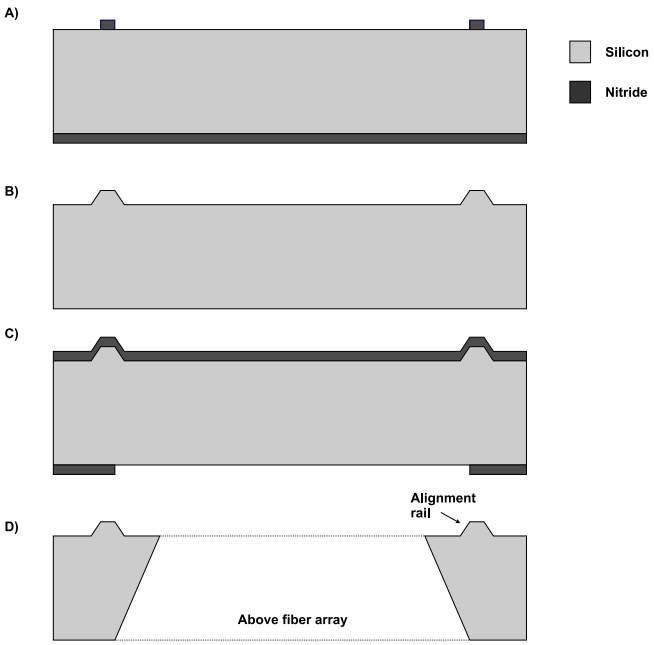


Figure 5.14: Process step for fabrication of the top plate. A) Alignment rails are defined are etched into the nitride layer. B) The alignment rails are etched in KOH and the nitride removed. C) The alignment rails are protected with nitride and a backside pattern is etched. D) KOH etch though the whole wafer from the backside to open the fiber array recess.

5.5 Summary

In this chapter the fiber pigtailing method developed in this project has been described. The method aims to work as a passive alignment technique. The pigtailing method involves fabrication of a planar waveguide substrate and a fiber array on which alignment trenches are integrated. The two arrays are assembled with a top plate on which the alignment rails fits into the alignment trenches on both the waveguide and the fiber substrate.

The advantages of the methods are: the mask writing process provides the horizontal alignment for all the three parts, the vertical alignment accuracy of the top plate and the fiber array carrier is insensitive to systematic offsets of the line width, and it is possible to test the performance of the waveguide chip before pigtailing. Finally, the use of batch processes potentially makes it a low cost method.

Chapter 6

The waveguide chip

A fabrication process of planar waveguide components integrated with alignment trenches for aligning the fiber array has been developed in this work. The fabrication process for planar waveguides in silica on silicon has been discussed in chapter 3. This process has been expanded with some additional processing steps to fabricate the alignment trenches. The principle of the fiber pigtailing method has been discussed in chapter 5. The process scheme is shown schematically in figure 5.1.

In section 6.1 etching of the waveguides is discussed. The fabricated waveguides have been measured before pigtailing with optical fibers. The measurements have led to making changes in the fabrication method to achieve low loss waveguides. This is discussed in section 6.2.

6.1 RIE etching of glass

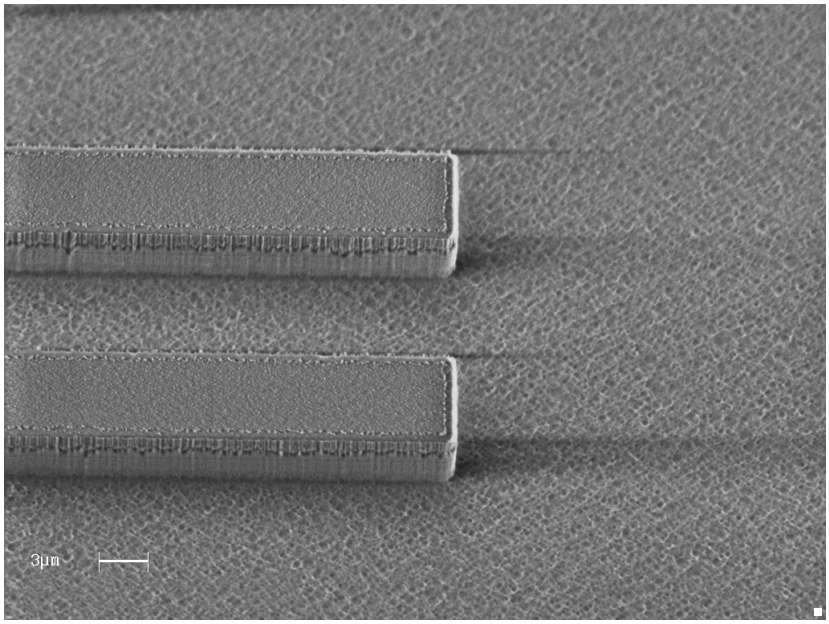
Etching the core is one of the critical process steps in the waveguide fabrication. In this step the waveguide cross section and sidewall roughness are determined. Both will have an influence on the optical quality and functionality of the waveguide.

In RIE etching it is possible to obtain both isotropic and anisotropic etching profiles of the core. RIE etching is a combination of three different etch mechanisms: Chemical etching, physical etching and ion assisted chemical etching. Chemical etching is a chemical reaction that occurs on the surface resulting in a volatile product. Pure chemical etching is isotropic. Physical etching is caused by ion bombardment of the surface which removes the material by sputtering. Since most of the bombarding ions are incident perpendicular to the surface, sputtering mainly occurs anisotropic. In the ion assisted chemical etch the highly energetic ions contribute with energy for the chemical reaction to occur. Which of the three mechanisms dominates a particular etch process can be controlled with the chamber pressure and the applied RF power [28]. Silica can be etched in plasmas that produce fluorine atoms or with gases that generate unsaturate-rich fluorocarbon species CF_X [37]. Silica is etched very slowly by a spontaneous chemical reaction with atomic flourine, but the etch rate can be enhanced by ion bombardment. The etching of silica therefore inherently has a large degree of anisotropy [28].

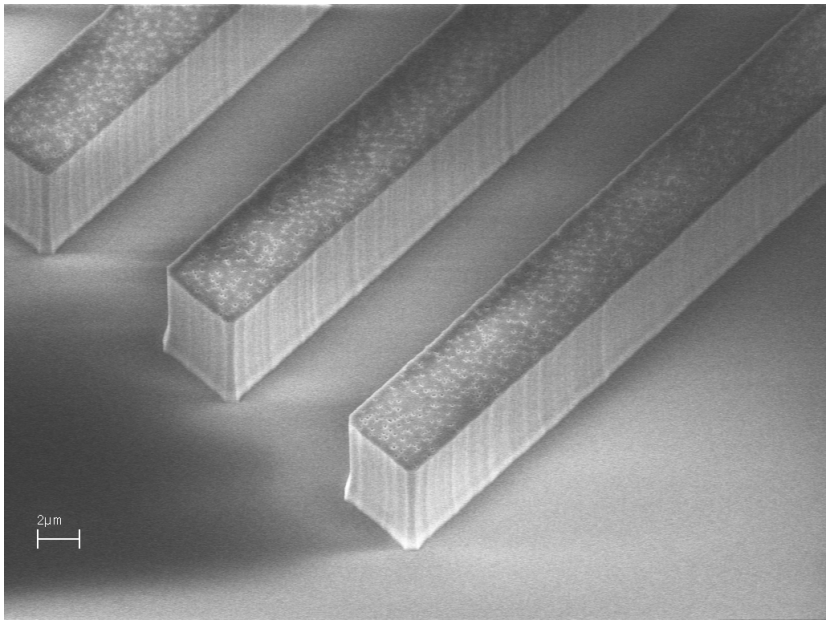
High sidewall roughness often appears in the RIE etch. This is severe since roughness in the central part of the core, where the field intensity is high, will result in high propagation loss. We have studied, if the sidewall roughness depends on the employed etch mask material. Two etch experiments have been performed, one using sputtered amorphous silicon and one using LPCVD polysilicon as etch mask material. The outcome of the two etch experiments is shown in figure 6.1. Both the waveguide sidewall and the wafer surface are rough when using sputtered amorphous silicon as etch mask. Using LPCVD polysilicon yields much smoother waveguide sidewalls and wafer surfaces than using sputtered amorphous silicon. Comparing the two types of silicon in an optical microscope clearly indicates that the sputtered amorphous silicon has a rougher surface than the polysilicon layer. The quality of the available sputtering equipment is apparently not good enough to achieve a good waveguide quality.

Another important feature of the etched cores is the geometry of the cross section. Optimization of the top cladding process at IONAS have made it possible to fill gaps between waveguides with vertical sidewalls. This cross section geometry is desirable since the core profile will be rectangular. If the sidewalls of the etched cores are angled it can cause higher polarization dependency due to the asymmetry with respect to the horizontal axis. Figure 6.2 shows a SEM picture of the core profile. The core profile is almost rectangular as preferred.

Both a good sidewall roughness and the desired cross section of the core have been obtained on the etched wafers. The reduction of the line width on the test wafers was around 0.8 μm, which is in the same process range as expected. However, when fabricating the first component wafers the line width reduction of the waveguides suddenly was much larger around 1.4 μm. This will make the core much smaller than expected and hereby alter the waveguide performance. The instability of the RIE etch could be caused by the high number of different processes run on the equipment. Due to the un-stability the component wafers were processed by another RIE equipment, which was only used for glass etch. This equipment was set up to 5 inch wafers, while the fabricated wafers were 4 inch. A 5 inch wafer with a KOH-etched recess was used as carrier for the 4 inch wafers.



(a) Sputtered amorphous silicon as etch mask.



(b) LPCVD polysilicon as etch mask.

Figure 6.1: SEM picture of RIE etched waveguides with silicon used as etch mask.

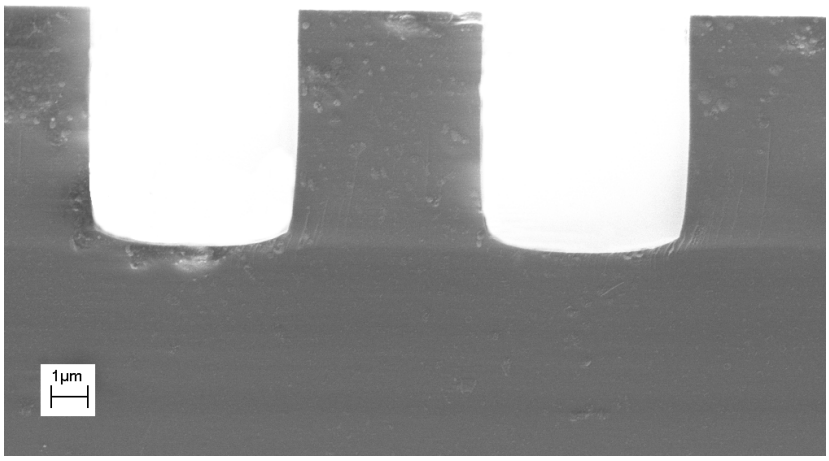


Figure 6.2: SEM picture of the facet of an etched wafer.

6.2 Loss measurements

The fabricated waveguide samples have been evaluated by measurements of the insertion loss (IL) and the polarization dependent loss (PDL). The central part of the setup is a five axis planar waveguide manipulator and two three axis stages with submicron precision for coupling light in and out of the waveguide. Reflections at the fiber-air-waveguide interface are reduced with a drop of refractive index matched oil. A calibration of the measurements is done by measuring the fiber-fiber loss before insertion of the waveguide sample. Subtracting the loss measured for coupling directly from the input to the output fiber yields an absolute value for the attenuation across the sample waveguide. The insertion loss measurements have primarily been done with a narrow band DFB fiber laser at 1546 nm as light source.

A single-mode waveguide supports two orthogonal polarization modes. Polarization dependency arises when the optical signal does not have the same guidance properties in the two polarization modes. Polarization dependent losses are in general an unwanted effect and subject to minimization. If the waveguide were symmetrical, with respect to both the horizontal and the vertical axes, no polarization dependent loss would occur. In reality a planar optical waveguide will be asymmetric due to anisotropic stress in the glass and sidewall roughness. Measurements of PDL are done by changing the polarization of the input light randomly over all possible states. The maximum insertion loss variation, when excited by all possible polarization states, are defined as PDL of a device.

Two kinds of waveguides have been fabricated, so-called low-delta waveguides and high-delta waveguides. They differ in the refractive index of the core glass. The refractive index difference between the core and the cladding is $\Delta n = 0.005$ for the low-delta waveguides and $\Delta n = 0.009$ for the high-delta waveguides, respectively. For each of the two types of waveguides two wafers have been fabricated: a fully processed

	Full process		**Reference process**	
Waveguide type	IL dB	PDL dB	IL dB	PDL dB
Straight waveguide	4.0	0.5	1.3	1.4
Bend waveguide	5.3	0.6	1.3	1.5

Table 6.1: Measurements of insertions loss (IL) and polarization dependent loss (PDL) on the low-delta waveguides.

	Fully process		**Reference process**	
Waveguide type	IL dB	PDL dB	IL dB	PDL dB
Straight waveguide	0.5	0.1	0.6	0.07
Bend waveguide	0.6	0.1	-	-
Splitter	4.85	0.25	-	-

Table 6.2: Measurements of insertion loss (IL) and polarization dependent loss (PDL) on high-delta waveguides.

wafer and a reference wafer. The reference wafer is made without the extra processing steps to fabricate the alignment trenches. All other processing steps are equal to the fully processed wafer. This is done to evaluate if the extra processing steps alter the waveguide performance.

Measurements on the low-delta waveguide samples are shown in table 6.1. The straight waveguides on the reference wafer has an insertion loss of 1.3 dB and a polarization dependent loss of 1.4 dB. The results are considered to be a high insertion loss and PDL. This is consistent with the performance of the variable optical attenuator (section 3.4). In general low-delta waveguides have shown high losses using this particular process scheme. The process scheme have been developed to be used for high-delta waveguide processing. The process scheme is clearly not compatible with the low-delta waveguides. The light is loosely confined is the core of a low-delta waveguide. Any changes in the index profile of the waveguide might effect the guidance. A change of the refractive index profile of the waveguide could be the explanation on the poor waveguide properties of the low-delta waveguides processed in this project.

The measurements of the high-delta waveguides are shown in table 6.2. Only straight waveguides have been measured on the reference wafer since the wafer broke during final inspection. The straight waveguides on both the reference wafer and the fully processed wafer has an insertion loss of 0.5 and less than 0.1 dB PDL. It can be concluded that the high-delta waveguide performance is good.

The insertion loss is a sum of the fiber to waveguide coupling losses and the propagation loss. Since the core refractive index of the high-delta waveguides is higher than in a standard optical fiber coupling loss between the waveguide and the optical fiber is a high percentage of the measured insertion loss. In chapter 4 the mode-mismatch loss was estimated to 0.48 dB pr. coupling. Based on the measurement this estimate

of the mode-mismatch loss is clearly too high, this indicates that the refractive index profile of the fabricated waveguides is not a squared step profile. This supports the explanation of the poor performance of the low-delta waveguides.

From table 6.2 it is seen that there is an excess loss of the splitters of approximately 1.4 dB. Inspection of the splitters in an optical microscope shows that residues are left in the region where the two arms of the splitter are close. This may be caused by either residues of the polysilicon layer or the photolithography step.

Another conclusion can be drawn from the measurements on the low-delta waveguides (table 6.1). The straight waveguides on the fully processed wafer has an insertion loss of 4.0 dB and a polarization dependent loss of 0.5 dB, which is an even higher insertion loss than on the reference wafer. Consequently, the extra processing of the alignment trenches is affecting the performance of the waveguides. This has been be solved by altering some of the processing steps. The processing changes is considered to be confidential information and is therefore not included in this thesis. The measurements on the high-delta waveguides (table 6.2) show that the insertion loss and PDL of the fully processed wafer and the reference wafer are comparable. It can be concluded that the altered processing step to fabricate the alignment trenches does not have any influence on the waveguide properties.

6.3 Summary

Experiments with different etching mask materials for the RIE etch of the cores are evaluated. Using sputtered amorphous silicon leads to higher surface roughness than using LPCVD polysilicon.

Measurements on the finished waveguide samples have been performed. The low-delta waveguides have both high insertion loss and polarization dependent loss. This is caused by using a process scheme optimized for another core refractive index. The high-delta waveguides have shown insertion loss at 0.5 dB and 0.1 dB polarization dependent loss. Hence, the high-delta waveguides are performing properly. Furthermore, it can be concluded that it is possible to add the fabrication of the alignment trenches without affecting the waveguide properties.

Chapter 7

Fiber array carrier and top plate

The uniformity of the KOH etch process across the whole four inch wafer is very important since it determines the alignment accuracy in the pigtailing process. The tolerance of the transverse fiber misalignment is of the order of 1 μm. Consequently, the widths and thereby the depths of the KOH etch of all the fiber V-grooves and alignment rails on the top plate have to be processed within that tolerance.

In chapter 5 the process schemes for both the fiber array and the top plate are explained. Hence, the purpose of this chapter is to evaluate some of the details of the processing steps used in the fabrication. The KOH etching process is a 28 wt.% solution at 80 $^\circ$C. This is a commonly used KOH etch configuration. For an introduction to the mechanism behind KOH etching see Seidel [38] and Elwenspoek [39].

The pattern of the KOH etched substrates has to be aligned to the crystal plane of the silicon wafer. This is discussed in section 7.1. In section 7.2 a short description of the photolithography steps is given. An important factor to achieve a good uniformity is the etching of the KOH mask material, which is discussed in section 7.3. Finally, in section 7.4 the final width of the processed component parts are evaluated.

7.1 Alignment to the silicon crystal plane

The major flat of a standard wafer is typically indicating the crystal direction with an accuracy of $\pm 1^\circ$. However, the dimensions of fiber V-grooves, the alignment trench, and the alignment rail are best controlled when the mask is perfectly aligned to a {110} direction [40]. Several methods have been proposed to align mask patterns to crystal orientation [41, 42, 43]. The alignment is most commonly done by etching test structures into the wafer revealing the {110} planes. The etched structures can then be used for alignment of the following mask patterns with a higher precision than when using the major flat of the wafer.

The method used in this project has been suggested by T. Storgaard-Larsen and has originally usually been used for revealing {111} planes on a {110} oriented wafer [44]. The pattern has two blocks of 100 lines, each 6 μm wide and 3 mm long and rotated with respect to each other in steps of 0.05°. The line patterns, symmetrically covering a 5° range around the center line parallel to the flat, are anisotropically etched into

the substrate in a radial distance of 4-4.3 cm from the center of the 4" wafer. In this project the pattern has been adopted to reveal the {110} plane on a {100} oriented wafer. A schematic view of the etched alignment pattern is shown in figure 7.1. The line which corresponds to the {110} plane of the wafer will remain on the wafer with the same width as on the mask. Misalignment to the crystal plane will show in an underetch of the line. Most of the line will be removed in the etching process. The line in the center of the remaining lines is parallel to the {110} crystal plane of the wafer within 0.05°.

A SEM picture of the etched alignment pattern is shown in figure 7.2. After 3 hours of KOH etching only around 10 lines are remaining in each of the alignment blocks. The rest is etched away due to misalignment to the {110} plane. However, due to problems in the following photolithography step the etching time of alignment mask have been reduced to 1 hour. Using this etching time around 20 lines are remaining in the alignment blocks. To determine which line may be used in the following alignment process an evaluation of the pattern has to be performed in an optical microscope.

7.2 Photolithography

For processing of the top plate substrate a problem arose in the second photolithography step (i.e. masking of the alignment rails). The alignment mark for the third mask (backside etch) is placed on the outer side of the two alignment blocks for the crystal orientation alignment. When spinning a standard 1.5 μm photoresist layer the photoresist was not covering the outer side of the alignment blocks. Consequently, the alignment marks for the third mask was missing.

Several solutions of the problem have been investigated: First, the etching time of the alignment blocks was lowered to decrease the depth of the holes. Secondly, the photoresist was dispensed both in the center of the wafer and at the radius of the alignment blocks. Third, another photoresist with a larger viscosity was used. Finally, spinning two layers of photoresist on top of each other was investigated.

Lowering the etching time of the alignment blocks did not improve the result. Neither did the experiment with dispensing the photoresist twice. Hence, it is not only the depth of the holes but also the surface tension around the alignment blocks that makes the photoresist unable to stick.

Using a high viscosity photoresist did solve the problems with the alignment marks. However, it was not considered useful since the process was difficult to reproduce. The thick photoresist is very dependent on the humidity in the room while spinning and exposure of the wafer. Bubbles occurred in the photoresist, while exposing the pattern. The bubbles destroy the quality of the photoresist pattern.

The uniformity of the double spin layer is not as good as in a standard photoresist spin. The photoresist did cover the outer side of the alignment blocks. Using a double spin process for a photolithography step, where the line width have to be controlled carefully, is not the best solution. Non-uniformity of the resist thickness will result in differences in the line width transfer.

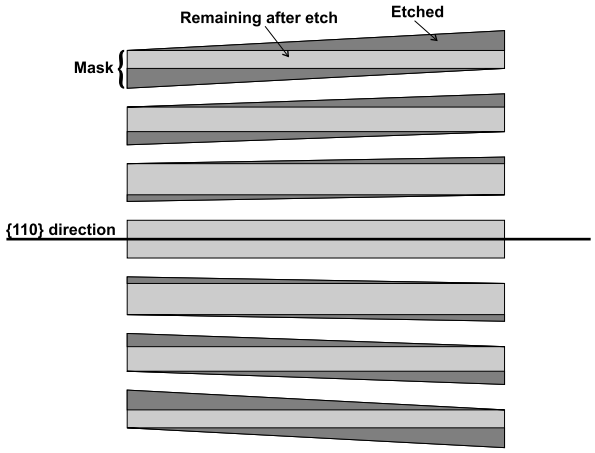


Figure 7.1: Schematic view of the mask for revealing the {110} planes of the wafer.

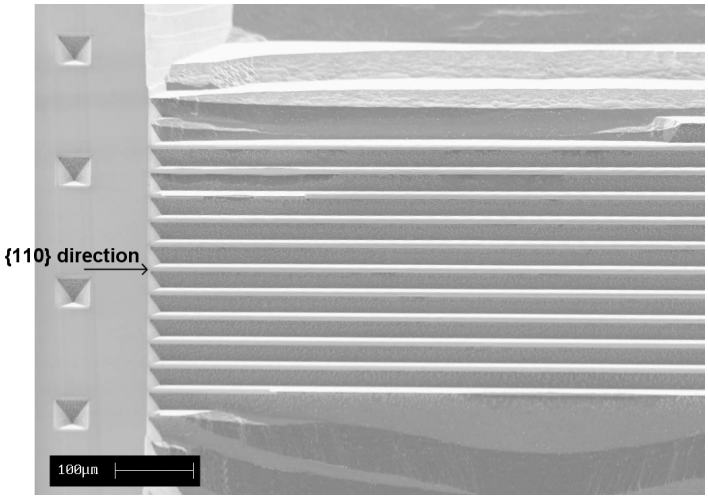


Figure 7.2: SEM picture of KOH etched alignment pattern (etching time 3 hours).

None of the investigated solutions are perfect. However, measurements on the final processed wafers have shown that the double spin solution is acceptable for this application. In further work a new mask where the alignment marks are moved to the inside of the crystal orientation alignment blocks is highly recommended.

7.3 Silicon nitride etch

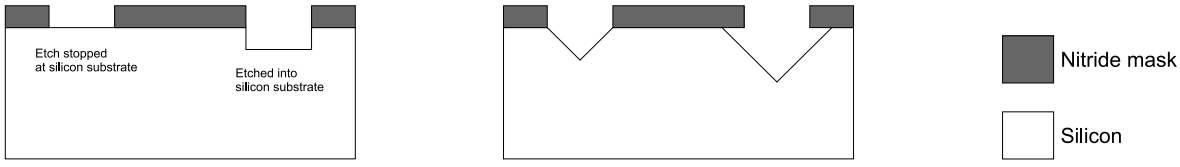
As KOH etch mask material either thermal oxide or silicon nitride is commonly used. Silicon nitride is much less attacked by KOH etching than thermal oxide. The etch rate is so small that it has not been determined yet [38]. The etch rate of thermal oxide can be as high as 100 nm/min [39]. Using thermal oxide as an etch mask could affect the line width of the etched structures due to the erosion of the mask. Silicon nitride (denoted nitride) has been chosen as etch mask in this project.

To obtain a good uniformity of the line width across the wafer the etching of thee nitride mask has to stop at the interface between the nitride layer and the silicon wafer. Etching into the silicon wafer at some places on the wafer will result in an under-etch of the nitride mask in the KOH-etch. The scenario is sketched in figure 7.3.

Two kinds of nitride etch have been investigated in this project. A dry RIE etch and a wet etch by phosphoric acid.

The RIE etch process used in this project is based on SF_6 and O_2. The process will also etch silicon even with a higher etch rate than the etch rate of nitride. Avoiding a non-uniform etch into the silicon wafer could be obtained by either a stop layer of thermal oxide beneath the nitride layer or a very uniform etch rate of the nitride mask. Using a thermal oxide stop layer could result in another problem with the line width due to erosion of the oxide mask in KOH. This possibility has not been investigated in this work. The uniformity of the nitride etch rate will depend on the process parameters. The strict requirements for the line width uniformity after the KOH-etch impose an etch depth uniformity of the nitride etch better than 5 %.

To investigate the uniformity of the RIE nitride etch experiments with different RF power and chamber pressure were carried out. In the experiments the mass flows were kept constant of 50 sccm SF_6 and 13 sccm O_2. The chosen etch parameters are listed in table 7.1.



(a) Substrate after nitride etch.

(b) Substrate after KOH etch.

Figure 7.3: Under-etch of nitride mask. At the right pattern the etch is continued into the silicon layer.

Process Parameters		**Etch Data**			
Power W	Pressure mTorr	Bias V	Mean etch rate Å/min	Selectivity resist/nitride	Uniformity %
30	80	46	307	1.70	16.3
30	100	37	308	1.62	21.6
30	120	33	291	1.92	26.6
45	80	80	558	1.57	16.0
45	100	54	474	1.49	20.7
45	120	43	469	1.62	13.5
60	80	108	807	1.38	10.9
60	100	84	710	1.52	23.1
60	120	64	668	1.50	27.0

Table 7.1: Process parameters and measured results from the nitride etch investigation.

Wafer preparation: Lightly doped four inch wafers were used in the experiment. The wafers were cleaned in a standard RCA cleaning process and a silicon rich nitride of 1250Å was deposited using LPCVD. The wafers were treated with HMDS and 1.5 μm of photoresist was spun and patterned through a standard photolithographic process. The pattern used was the same as for etching the alignment rails of the top plate. This was chosen to have the same load during the RIE experiments as in the actual processing.

RIE chamber condition: Cleaning and preconditioning of the etch chamber was performed before each etch. The chamber was cleaned by an oxygen plasma for five minutes followed by 5 minutes preconditioning with the process used for the specific experiment. Both cleaning and preconditioning were performed on a dummy silicon wafer. The silicon nitride etching time was 1 min for all processes.

Measurements: The step height of the structures was measured in 10 positions on each wafer using a TENCOR Long Scan Profiler. Measurements were performed on the photoresist pattern, after etch i.e. both remaining photoresist and nitride etch, and after removal of the photoresist in acetone. The two first measurements were performed to be able to determine the selectivity to photoresist in the nitride etch process. The repeatability on the measurements is around $\pm$ 20 Å.

The selectivity to resist is listed in table 7.1. The listed values are the mean value across the wafer. All the etch processes have a slightly higher etch rate of photoresist than nitride. However, since the photoresist thickness is at least 1.5 μm and the nitride layer 1500 Å this will not cause any problems in the nitride etch.

The mean value of the etch rates across the wafer are listed in table 7.1. An example of a measured etch depth data as a function of location on the wafer is shown in figure 7.4. The fitted line is a second order polynomial fit. The experiment was in the middle of the process parameter range with a pressure of 100 mTorr and power of 45 W. The variation of the etch depth with respect to the radial distance from the center of the

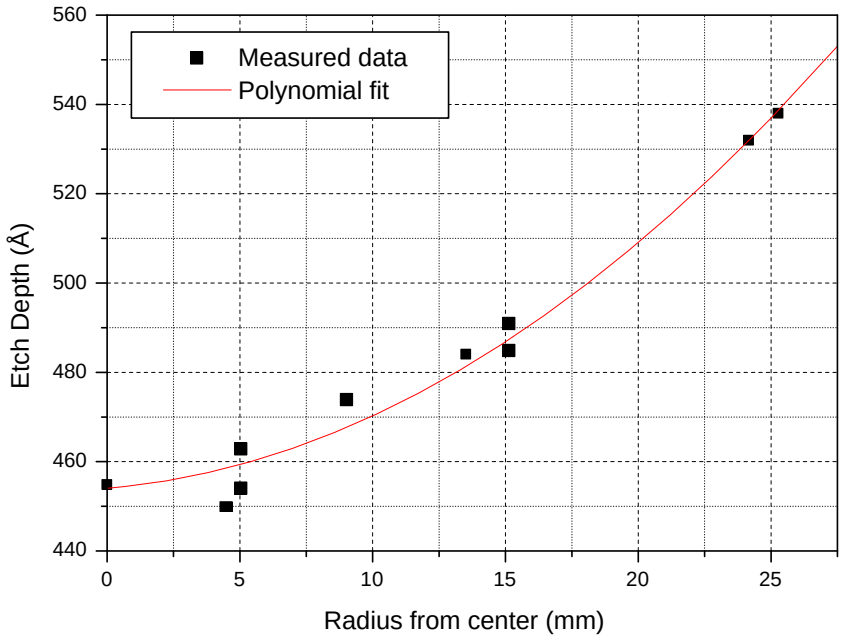


Figure 7.4: Measured etch depths of nitride as a function of the radial distance from the wafer center.

wafer is typical for all of the measured processes. All the measured wafers show an increase in etch rate towards the edge of the wafer.

The measured uniformity is given in table 7.1. The uniformity is calculated as follows: The difference between the maximum and minimum etch rate divided by the value in the center of the wafer. The data is normalized to the center value in order to be able to compare the uniformity despite the differences in the overall etch rate. In the table it can be seen that the uniformity changes from 10 - 27 % in the explored process parameter range. The investigated process parameter range of the RIE etch did not provide an etch with a uniformity below 5 %. Consequently, the RIE etch was not considered as a good solution to the nitride mask etch. However it should be noted that using another gas chemistry would be another possibility. Un-saturated fluorine-deficient plasmas using for example CHF_3 as feed gas anisotropically etch both nitride and silica with high selectivity over silicon [37]. Hence, this gas chemistry could be a better choice for etching the nitride mask than the current.

Another possibility to stop the nitride etch at the silicon surface is to use a phosphoric acid wet etch. The mask for the nitride etch is provided by thermal oxidation of the nitride layer. Hereby, the surface of the nitride layer is converted into silica. This very thin oxide layer is patterned in BHF and serves as etch mask for the subsequent structuring of the nitride layer in phosphoric acid at 180 $^\circ$C [45]. The phosphoric acid has a high selectivity to silicon the etching is stopped very precisely on the silicon

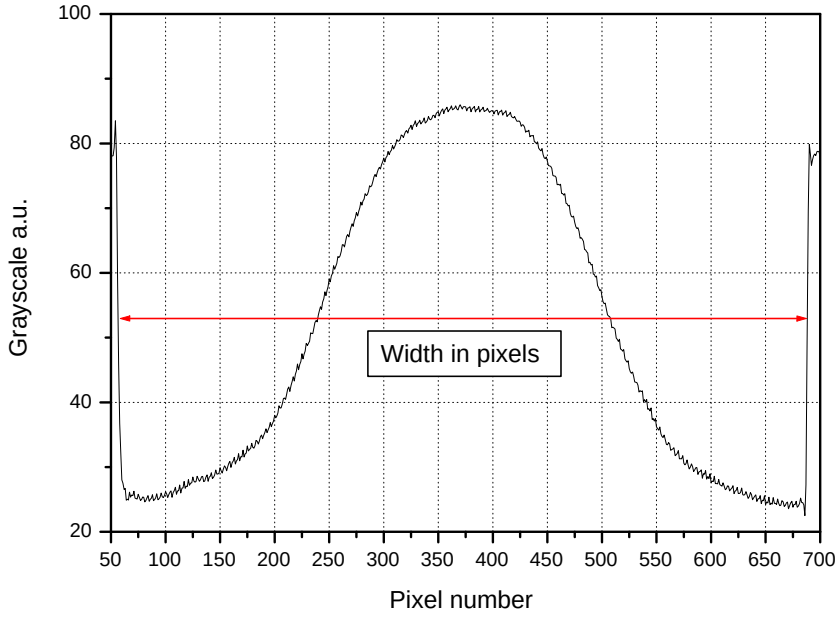


Figure 7.5: Gray scale values as a function of the pixel value across a V-groove.

layer. The nitride etch rate in hot phosphoric acid is quite low around 10 nm/min. Consequently, the etch time is considerable longer compared to the RIE etch. However, considering production cost the wet etch have a advantage since it is a batch process. This latter solution for gaining a good etch stop at the silicon surface have been implemented. Based on the measurements on the line width uniformity this etching process is working well (see section 7.4).

7.4 Line width uniformity

Measurements of the line width on the finished fiber arrays and top plate samples have been done to evaluate the uniformity of the processed wafers. The measurements were done with an optical microscope with a frame grabber with 768x576 pixels. Each picture was taken with the highest possible magnification (x50 micro-objective) to achieve the best resolution of the measurements. The edge of the KOH etched structures can be seen as a step of the gray scale in the pictures. This is shown in figure 7.5. The width in pixels was measured as the distance between the middle of the two edges on the picture as sketched on the figure.

To achieve a real length in microns a calibration is needed. This is done by measuring with a x20 micro-objective, taken picture of two V-grooves at the same time. Since the distance between the V-grooves are known to be 250 μm this can be used calcu-

	Width on mask		**Measured date**	
Chip no.	V-groove μm	Trench μm	V-groove μm	Trench μm
1	178.37	35.61	179.75 ± 0.13	37.09 ± 0.16
2	178.67	35.91	179.90 ± 0.11	36.92 ± 0.03
6	178.37	50.61	179.84 ± 0.18	52.23 ± 0.04
8	178.97	51.21	180.63 ± 0.22	52.68 ± 0.17
11	178.37	80.61	179.57 ± 0.14	82.12 ± 0.03
14	179.27	81.51	181.12 ± 0.13	83.30 ± 0.02

Table 7.2: Measurements of the line width of the V-grooves and alignment trenches.

late the width of the V-grooves. A measurement of the same V-grooves with the x50 micro-objective has been used to calibrate the measurements. The absolute width with this calibration is not very accurate. Differences up to 0.5 μm measuring on the same grooves have been noticed. Also it can not be concluded that the measurements are done exactly on the top of the edge of the structures. However, since the measurements are performed on the same way on all the structures it can be used to determine the difference between the width of the V-grooves. As discussed in chapter 5 a systematic offset of the line width will not affect the alignment accuracy. Hence, the important information about the line width of the V-grooves is the difference between the widths and not the absolute value.

First an experiment was carried out to examine the measuring repeatability. Ten pictures of the same V-groove was taken. For each picture the focusing on the groove have been redone. The result gave a width of 181.1 ± 0.1 μm.

Measurements have been performed on six different V-groove chips. All 11 V-grooves and the two alignment trenches have been measured on each chip. The result can be seen in table 7.2. The standard deviation of the V-groove width is most commonly below $\sigma_v = 0.15$ μm, the maximum measured standard deviation is $\sigma_{v,max} = 0.22$ μm. Furthermore is the standard deviation of the width of the alignment trench is most commonly below $\sigma_{va} = 0.05$ μm, the maximum measured standard deviation is $\sigma_{va,max} = 0.17$ μm.

Measurements on the alignment rails have been performed on 15 top plate rails. The result can be seen in table 7.3. The standard deviation of the width of the two alignment rails on the same chip is most commonly below $\sigma_{ta} = 0.1$ μm, the maximum measured standard deviation is $\sigma_{ta,max} = 0.24$ μm.

The standard deviation of the misalignment in the total pigtailing process can be found using equation 5.2. Inserting the typical standard deviations the standard deviation is calculated to $\sigma = 0.17$ μm, using the maximum values the result is $\sigma_{max} = 0.33$ μm. In chapter 4 it was shown that a transverse misalignment of 1.0 μm corresponds to 0.2 dB coupling loss. Since both the typical standard deviation and the corresponding maximum value are significantly lower than 1.0 μm it can be concluded that the accuracy of the KOH etched substrates is adequate for the alignment process.

	Width on mask	**Measured date**		
Chip no.	Width μm	Rail left μm	Rail right μm	Width μm
1	7.33	6.38	6.32	6.35 ± 0.04
2	7.63	6.77	6.70	6.74 ± 0.05
3	7.93	7.01	6.96	6.99 ± 0.04
4	8.23	7.26	7.14	7.20 ± 0.08
5	8.53	7.51	7.52	7.52 ± 0.01
6	22.33	21.10	21.19	21.15 ± 0.06
7	22.63	21.51	21.33	21.42 ± 0.13
8	22.73	21.69	21.68	21.69 ± 0.01
9	23.23	21.95	21.85	21.90 ± 0.07
10	23.53	22.38	22.31	22.34 ± 0.05
11	52.33	50.89	50.93	50.91 ± 0.03
12	52.63	51.20	50.89	51.05 ± 0.22
13	52.93	51.42	51.40	51.41 ± 0.01
14	53.23	51.89	51.89	51.89 ± 0.0
15	53.53	51.96	52.30	52.13 ± 0.24

Table 7.3: Measurements of the line width of the alignment rails on the top plate.

7.5 Summary

A KOH-etch mask alignment scheme has been adopted. The precision of the alignment of the mask pattern to the crystal orientation of the silicon substrate is within ± 0.05 $^\circ$.

The patterning of the silicon nitride mask has been studied in detail. The investigated RIE etch yields insufficient uniformity of the silicon nitride etch rate to be adequate for this application. Instead a wet etch using phosphoric acid has been implemented with good results.

The final measurements on the KOH etched structures showed a typical standard deviation of 0.15 μm on the fiber V-grooves, 0.05 μm on the alignment trenches, and 0.1 μm for the alignment rails. The standard deviation of the misalignment in the total pigtailing process is calculated to 0.17 μm. It was concluded that the uniformity of the etched structures is adequate for the pigtailing process.

Chapter 8

Dicing and polishing

After processing the waveguide wafer is diced into chips. A smooth facet of the waveguide chip is important in order to obtain a low coupling loss and low reflection. A smooth facet of the chip is usually obtained by polishing. In order to minimize the need for polishing a good dicing process is important. The smoother the facet is after dicing the easier the polishing process is since less material has to be removed.

In this project both a new dicing process and a polishing process are developed. In section 8.1 the dicing process is described. Both the choice of dicing blade and the dicing process parameters are evaluated. The developed polishing process is discussed in section 8.2.

8.1 Dicing

All optimization of the dicing process has been done on a MicroAce 3 from Loadpoint. Before dicing the substrate is mounted on a ring mount with tape. The tape most commonly used is a P.V.C. sheet with an adhesive applied to the top side of the tape. The tape makes it possible to dice through the substrate into the tape.

To obtain a good dicing process it is important both to select the correct blade and adjust the dicing parameters on the dicing saw. The first dicing experiment was done with the standard blade and process parameters used at Mikroelektronik Centret. The blade is a plated diamond blade, with a width of 45 μm, exposure 1.08 mm and with a size of the diamond particles of 4-6 μm. A SEM picture of the diced facet can be seen in figure 8.1. As it can be seen from the picture the facet is not smooth. The facet of the silicon wafer is rippled and parts of the glass are chipped off. When inspecting the upper side of the chip in an optical microscope it can be seen that the glass is chipping off.

Two common types of dicing blades are used in the micro electronic industry. A plated diamond blade, in which the diamond particles are held in a nickel bond. And a resinoid diamond blade, in which diamond particles are held in a resin bond to create a homogeneous matrix. Silicon wafer dicing is usually done with the plated diamond blade. The resinoid diamond blade is usually used in hard materials as sapphire, aluminum and quartz. The resin blade sharpens itself during cutting, since the diamond

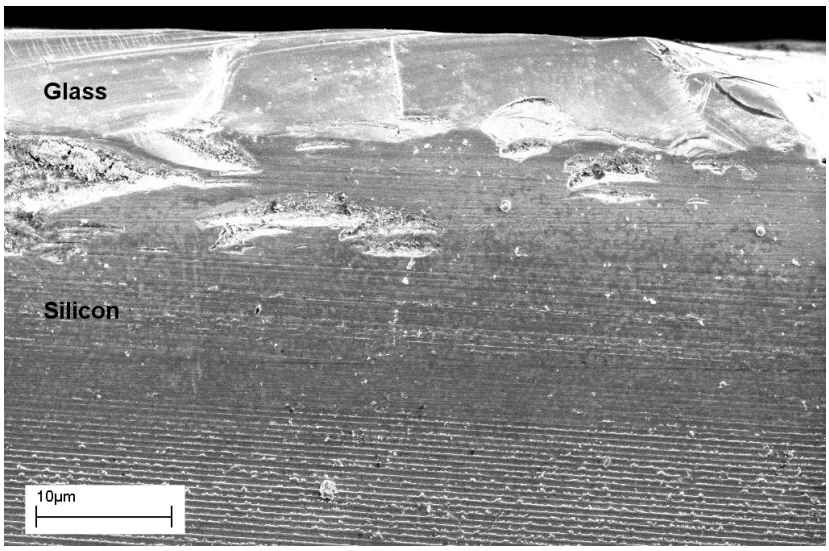
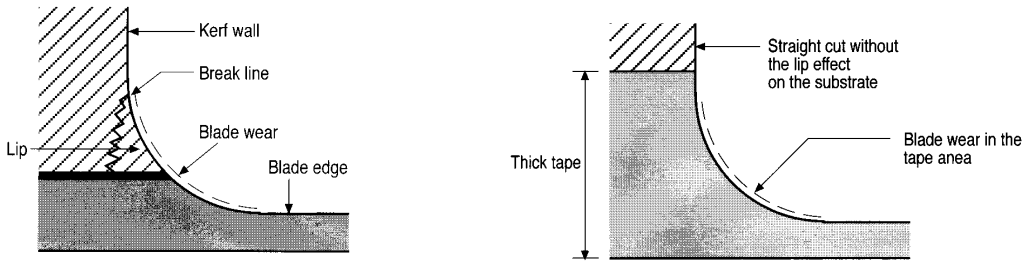


Figure 8.1: SEM picture of diced facet using the originate dicing blade and dicing parameters.

particles pull loose from the blade. Hence, exposing a new sharpened edge. However, the life time of the blade is much shorter compared with a nickel blade. The diamond particle size is also important when selecting the blade. Due to the hardness of glass it is normally recommended to use diamond particles around 30-45 μm for this material. However, since the smoothness of the facet is very important in this case the diamond size chosen was only 15 μm. This will also lower the life time of the blade.

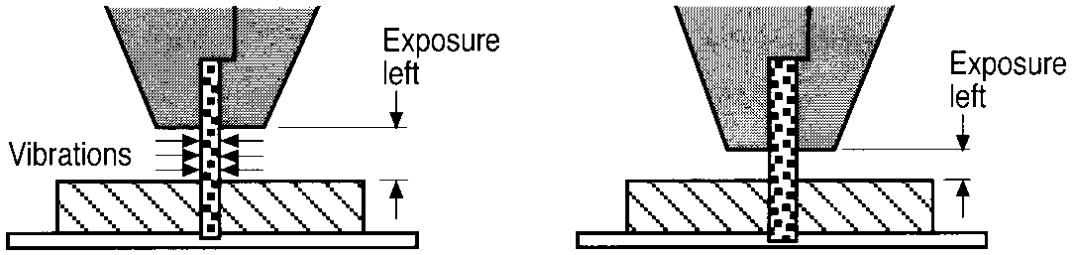
A problem frequently seen in the dicing process is chipping at the bottom of the chip, where the substrate is in contact with the tape [46]. This can be caused by air gaps between the substrate and the tape, which should be eliminated if possible in the mounting process. When using a resinoid blade the chipping is mainly caused by high blade wear. Blade wear mainly occurs at the blade edge, which become rounded during cutting. This causes a small lip on the substrate at the contact point with the tape. The lip breaks off the substrate either during cutting or while dismounting the chips. A schematically view of this is shown in figure 8.2(a). Cutting deeper into the tape will eliminate the lip effect. This is shown schematically in figure 8.2(b). The chip will have a straight edge and the round part of the blade edge will be inside the tape. Since the dicing blade will become smaller during use it is important to calibrate the cut depth regularly. On the used dicing saw this can be done using a zero calibration button, which is located outside the cutting area. Hence, it is possible to make a height calibration after any number of cuts, without the need of taking the substrate of the dicing saw.

Another problem commonly seen in the dicing process is chipping and large cracks on the top of the substrate. This is mainly caused by chip movement during the cutting process [46]. Several parameters does influence on this. If the tape adhesion is not strong enough it can cause the chip to move during cutting. Lowering the dicing feed rate will also decrease the amount of chipping. Furthermore, the amount of chipping



(a) Chipping. (b) No chipping.

Figure 8.2: Chipping caused by high blade wear (from ref. [46]).



(a) Thin blade (b) Broad blade

Figure 8.3: Vibrations caused by cutting with a thin blade with large exposure (from ref. [46]).

can be caused by vibrations in the dicing blade. If the blade is thin and the exposure large vibration of the blade can occur. This is illustrated in figure 8.3(a). A solution to avoid this is to choose a dicing blade with a smaller exposure and or a thicker blade, see figure 8.3(b). This will lower the amount of chipping.

Taking all above into account another blade was chosen for the dicing process. A resinoid diamond blade with a width of 100 μm, an exposure of 1 mm and a diamond size of 15 μm has been chosen. Hence, the width of the blade is broader to reduce vibrations. The exposure of the blade is the same as in the initial experiment since the thickness of the wafer is almost 700 μm not leaving enough room to lower the exposure. The dicing feed rate is lowered to 0.05 inch/sec and the spindle rate of the blade 25,000 rpm. This have been chosen by visual inspection of the diced facets with different feed rates and spindle speeds. In figure 8.4 SEM pictures of the diced facet are shown. Compared to figure 8.1 it can be seen that the surface is much smoother than before optimizing the process. When inspecting the diced chip in an optical microscope almost no chipping is observed. The result of optimizing the dicing process is so good that it is not necessary to polish the final components before pigtailing.

In figure 8.5 a SEM picture of the bottom edge of a diced chip is shown. It can be seen that a small lip has broken off the chip edge. This is the scenario showed in figure 8.2(a). Hence, the depth of the cut is not selected large enough. However, by selecting a larger cutting depth this has been solved.

8.2 Polishing

Mechanical preparation is the most common method of obtaining a perfect finish of the waveguide facets. Mechanical preparation is divided into three operations: Grinding, polishing, and oxide polishing. Both grinding and polishing are material removal using fixed abrasive particles which produce chips of the sample material. The preparation is started with the smallest possible grain size to avoid excessive damage to the sample. During the subsequent preparation steps, the largest possible interval from one grain size to the next is chosen in order to minimize the preparation time.

The first steps of mechanical material removal are called grinding. Proper grinding removes damaged or deformed surface material, while introducing only limited amounts of new deformation. The aim is a plane surface with minimal damage that can be removed easily during polishing in the shortest possible time. The first grinding step is usually defined as Plane Grinding. Plane Grinding ensures that the surfaces of all specimens are similar, despite their initial condition and their previous treatment. In addition, when several specimens are polished together, they must all be in the same plane for further preparation.

Like grinding, polishing must remove the damage introduced by previous operations. This is achieved with steps of successively finer abrasive particles. Diamond is used as an abrasive to accomplish the fastest material removal and the best possible planeness. Because of its hardness, diamond cuts extremely well through all materials.

The last step is oxide polishing. For glass waveguides, a combination of chemical and mechanical polish using a high-PH colloidal silica solution and a rubber pad works best. The colloidal silica has a grain size of approximately 0.06 μm and a PH of about 9.8. The combination of chemical activity and fine, gentle abrasion produces absolutely scratch free, deformation free specimens.

The samples are mounted in a special chuck for hand polishing of the samples. A picture of the polishing chuck is shown in figure 8.6. A minimum of two samples are polished together mounted with the glass side against each other. This is done to avoid edge effects on the polished samples. In some of the experiments the two samples are mounted without any material between the samples. In other experiments the two samples are waxed together before mounting in the polishing chuck.

As it can be seen in figure 8.6 four quartz rods are mounted on the polishing chuck. If the pressure on the chuck is uniform while polishing, the quartz rods ensures that the polishing on the chip will be perpendicular to the waveguides. When mounting the samples the quartz rods on the chuck is standing on a piece of brass. This way the samples will stick out longer than the quartz rod. The side of the samples is aligned to one of the sides of the sample recess. This ensures that the polishing is done

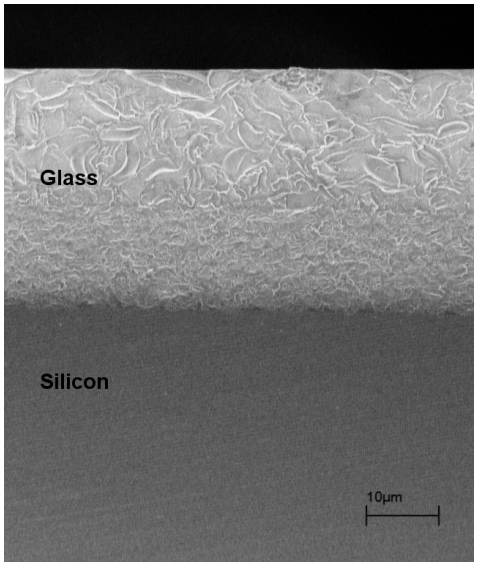


Figure 8.4: SEM picture of diced facet using an optimized dicing process.

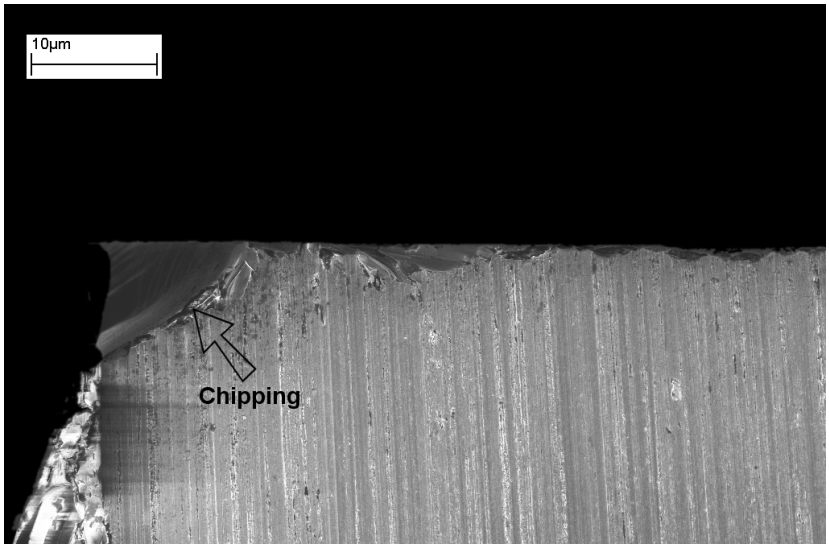


Figure 8.5: SEM picture of the bottom edge of a diced chip.

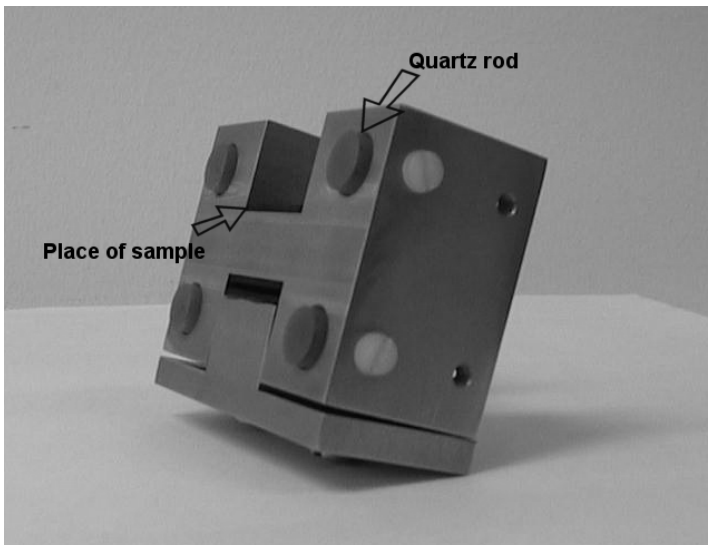


Figure 8.6: Hand held polishing chuck.

perpendicular to the waveguides.

The chosen process steps are listed below:

- **Plane Grinding:** 30 μm
- **Polishing Step 1:** 12 μm
- **Polishing Step 2:** 3 μm
- **Polishing Step 3:** 0.3 μm
- **Oxide Polishing:** MasterMet

A back plane microscope have been used to evaluate the result between each step of the process. The pad velocity of all of the step have been set to 150 rpm. If it was any larger it became difficult to control the polishing chuck by hand. While polishing, the chuck is turned slowly around in the opposite direction than the polishing pad. Plane grinding of the samples is done until the sample and the four quartz rods are in the same plane. This is achieved when all the surfaces have the same polishing finish. In the rest of the steps the polishing continued until it could be verified in the microscope that the lines from the previous step were removed. The oxide polishing has to be done really carefully. Since the sample is flat it might stick to the pad. If the polishing chuck is held loosely it may suddenly fly though the room.

In general it is important to clean the sample and the rods very carefully between each step. Otherwise polishing particles from the previous step may still be present creating large scratches in the next step. For cleaning the sample a toothbrush, hot water and dish soap are used.

Sufficient lubrication between the sample surface and the grinding/polishing surface is necessary. The correct lubricant improves the cutting process and yields the smallest

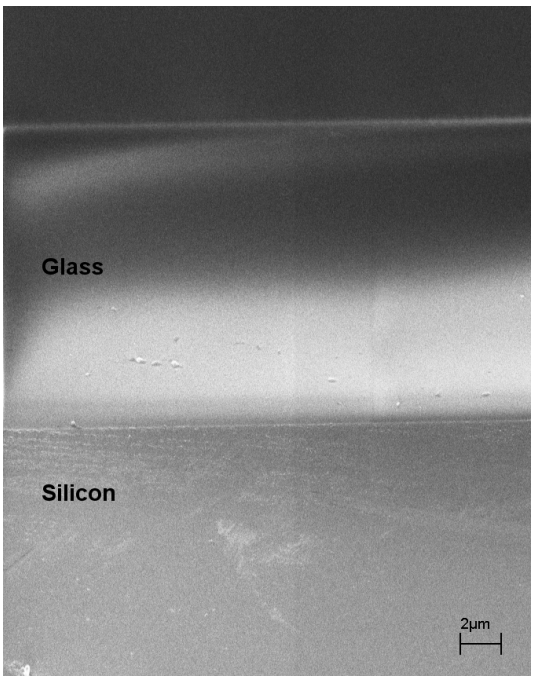


Figure 8.7: SEM picture of a polished buffer layer.

scratch depth and the lowest deformation. Secondly, the friction between the sample and the surface must be correct. Too little lubricant will cause overheating, too much lubricant will decrease the cutting action and creating a hydro-planning condition. Water is used as lubricant in all the polishing experiments done within this project.

The first polishing experiments were done on chips with only the buffer layer of glass (15 μm of thermal oxide). A SEM picture of the polished chip can be seen in figure 8.7. The facet of the chip is seen to be very smooth as expected.

Subsequently, polishing was done with a fully processed chip. The result is shown in figure 8.8. It can be seen from the picture that the top cladding is chipping off during the polishing process. When inspecting the samples in the back plane microscope during the process it is seen that the chipping of the top cladding is occurring in the plane grinding step. Two initiatives have been implemented to resolve this problem. The two samples polished at the same time have been waxed together with bee wax. This is done to avoid particles to penetrate into the space between the samples and thereby chipping of the top cladding. Secondly, the polishing time of the plane grinding step was lowered to 10 seconds. Cleaning of the polishing pad and the polishing chuck was done before continuing the plane grinding. This way large particles removed from the sample will not contaminate the polishing surface.

The two changes did decrease the amount of chipping. However, some chipping of the top cladding did still occur. This could be caused by air gaps between the sample and the mounting wax. To totally remove the chipping problem it is recommended to investigate other mounting materials and/or lower the size of the diamond particles in the plane grinding step. However, since the facet from the optimized dicing process is

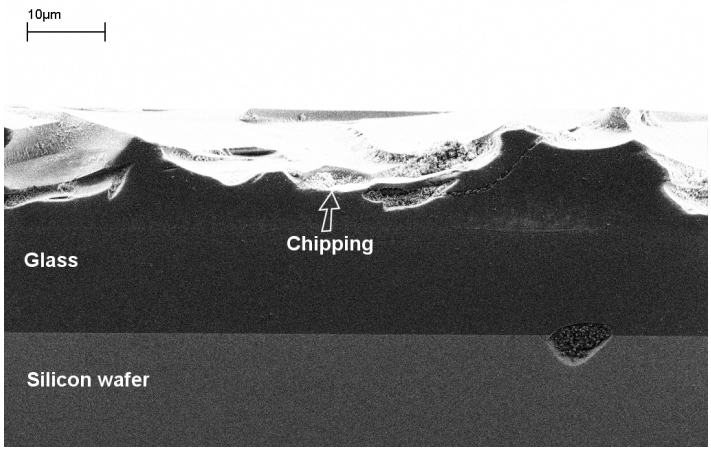


Figure 8.8: SEM picture of a polished waveguide component.

very smooth, it have been chosen not to investigate the polishing process further.

8.3 Summary

The dicing process have been optimized. Changing the blade to a resinoid diamond blade and adjusting the dicing parameters resulted in a perfectly smooth facet. The diced facet is so smooth that it have been chosen to use the diced waveguide samples without polishing.

A polishing process have been implemented. The result on polished samples only with a buffer layer is good. However, when applying the same process to fully processed chips, the top cladding is chipping off. The amount of chipping have been lowered but not totally removed. It is expected that the chipping can be avoided by using a smaller size of the diamond particles in the plane grinding step and another mounting wax.

Chapter 9

Pigtailing of components

Low-cost fiber pigtailing of integrated optical devices is a key issue in system applications. The primary cost of the components lies in their packaging because of the critical operation of the fiber pigtailing. In this work a new passive alignment technique has been implemented. The assembly consists of three parts, a fiber array, a waveguide chip and a top plate. The top plate is used to align the waveguide chip and the fiber array with respect to each other. The principle of the pigtailing method has been presented in chapter 5.

Mounting of the different parts and measurements on the pigtailed components are discussed in this chapter. In section 9.1 the method for mounting the fiber array is described. Connecting the waveguide sample and measurements on the devices are discussed in section 9.2.

9.1 Mounting of fiber array and top plate

In the assembly process the fiber array carrier, 11 fibers, and the top plate are glued together at the same time. When the fibers and the top plate are in the right position they are fixed by applying an adhesive. Since the assembly consist of a large number of different parts it is not practical to assemble it on a hot plate. Furthermore, the alignment accuracy could be destroyed if the assembly has to be moved before curing the adhesive. For this reason it has been chosen to work with an adhesive which is cured by exposure to UV-light. For mounting the fiber array and the top plate only the mechanical properties of the adhesive are important, since none of the adhesive will be in the light path. The chosen adhesive is Epotek OG198, which is a low viscosity (100 cps) commercial available adhesive. To achieve a good thermal stability of the adhesive the assembly is annealed on a hot plate at 150 $^{\circ}$C after the UV-cure.

9.1.1 Mounting process

Before the assembly all the parts are cleaned with isopropanol. The coating of the 11 fibers are stripped and then cleaned with isopropanol. The fibers are cleaved using a mechanical cleaver. The length of the un-coated fiber ends is 12 mm. The length

of the fiber array carrier is 10 mm. Hence, the fibers mounted in the V-grooves are un-coated. After assembling of the fiber array the un-coated fibers outside the fiber array carrier are protected with silicone. In a mass production it would be preferred to polish the fiber array instead of using cleaved fibers, since it is easy to scratch the fiber facet during the assembly. It is possible to do so with this pigtailing method. However, the top plate then has to be mounted separately.

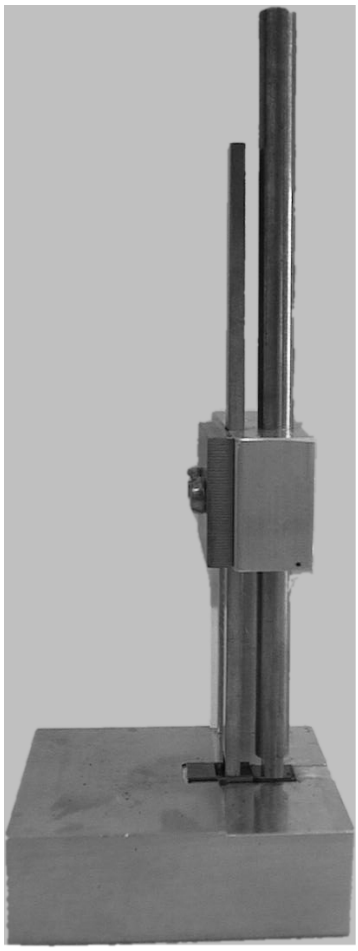
The assembly of the fiber array and top plate consist of a large number of different parts, which makes it necessary use an assembly tool. A picture of the assembly tool is shown in figure 9.1. The fiber array carrier is placed in the assembly tool and the top plate is placed above it with the alignment rails facing downwards. A rod is carefully placed pressing on the two alignment rails on the top plate. The top plate is moved slightly side wards until the alignment rails reaches the alignment trenches. A weight of 50 gram is placed on the rod to ensure that the top plate remains at its position. Finally, the top plate is slowly moved until the edge of the fiber array carrier and the edge between the alignment rails are above each other.

Subsequently, two of the optical fibers are inserted in the V-grooves, one in each side of the array. The fibers are held by a piece of tape. A piece of silicon is placed on top of the optical fibers and a rod is used to hold the fibers and the silicon pad. The silicon pad is diced from a standard silicon wafer. The wafer has been thinned in KOH to ensure that the upper surface of the fiber array is below the upper surface of the top plate. Which is important when mounting the waveguide sample to the fiber array. The tape, which was used to hold the two fibers while mounting, is subsequently removed. The remaining 9 optical fibers are carefully pushed from the end of the V-groove beneath the silicon pad. It is important not to scratch the fiber facet in the procedure, since a scratch would cause a high loss in the fiber to waveguide coupling. When all the optical fibers are placed correctly a weight of 100 gram is placed on the top of the rod. The fibers are pushed carefully forward until the fiber ends reached the end of the fiber array carrier. The upper third of the optical fiber will touch the edge of the top plate. This is used to place the optical fibers in the right longitudinal position. When inspecting the fiber array in an optical microscope after assembly, it was estimated that the fibers was placed in the right longitudinal position within $\pm$ 10 μm.

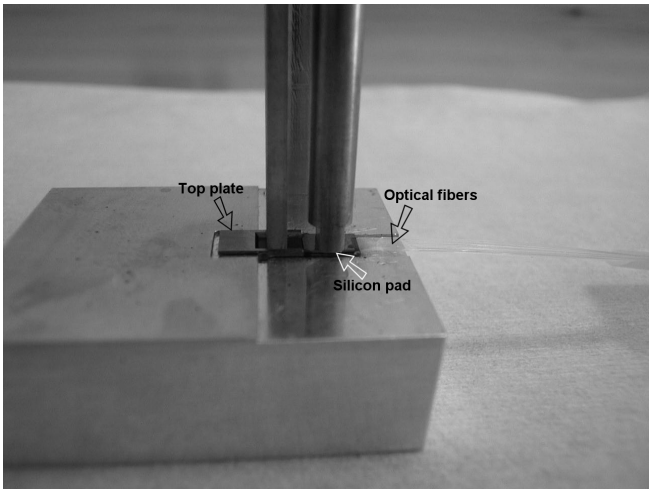
Finally, the adhesive is dispensed. A small amount of adhesive is placed at the end of the fiber V-grooves and the alignment trenches. Due to capillary forces the adhesive is sucked into the V-grooves and distributed evenly in the grooves. The adhesive is cured with an UV-light exposure in 2 minutes. Subsequently, the holder is moved to a hot plate and post baked at 150 $^{\circ}$C for 1 hour.

9.1.2 Evaluation of mounted fiber array

The 11 fibers and the top plate are assembled in the same step as explained in section 9.1.1. After the assembly it is impossible to investigate the alignment accuracy, since the top plate is covering the end of the fiber array. To investigate how good the assembly is some of the fiber arrays have been diced through. This makes it possible



(a) Total view



(b) Close-up

Figure 9.1: Assembly tool for the fiber array and top plate.

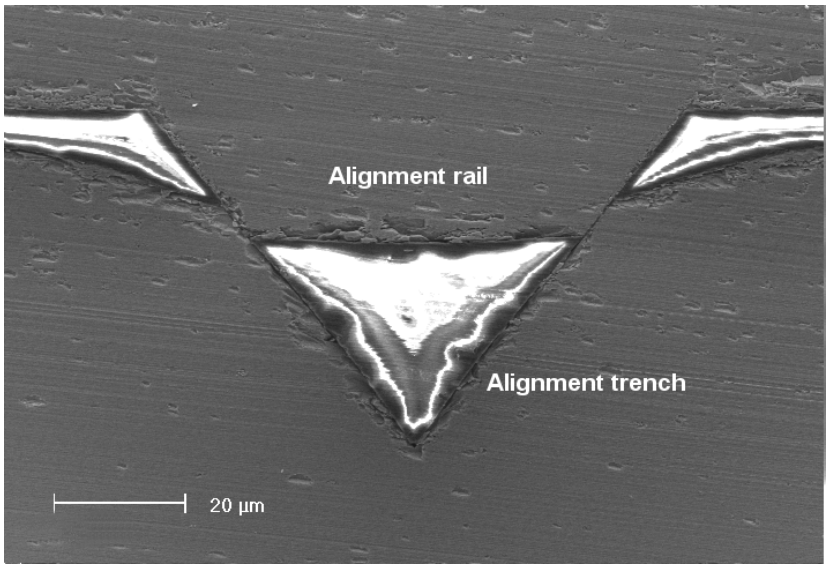


Figure 9.2: SEM picture of a correctly positioned alignment rail.

to evaluate both the positioning of the optical fibers in the V-grooves and positioning of the alignment rails in the alignment trenches.

In figure 9.2 a SEM picture of the alignment structures is shown. It can be seen that the alignment rail fits into the alignment trench. The edges of the structures fit perfectly together and there is no adhesive between the structures. This indicates that the alignment between the top plate and the fiber array carrier is good. This is seen to be the general case on most of the diced fiber arrays. However, the smallest alignment rails (corresponding to the 15 μm on the waveguide chip) did not always reach the right position in the alignment trenches. A SEM picture of a misaligned sample is shown in figure 9.3. The alignment rail is positioned on the top of the fiber array carrier instead of in the alignment trench. When placing the top plate into the fiber array carrier the correct position was determined by feeling the alignment rails getting into the alignment trenches. It will be more difficult to feel this when assembling the small structures. This is probably causing the higher amount of misalignment of the small alignment structures.

The correct position of all the 11 fibers are as important as the positioning of the alignment structures. In figure 9.4 a SEM picture of the fiber array facet with optical fibers is shown. The optical fiber is touching the V-groove edge at two points, which appears to be symmetrical with respect to the V-groove. A close-up of the fiber side touching the V-groove is shown in figure 9.5. No adhesive is seen at the spot where the fiber touches the V-groove. This indicates that the optical fiber is correctly positioned in the groove.

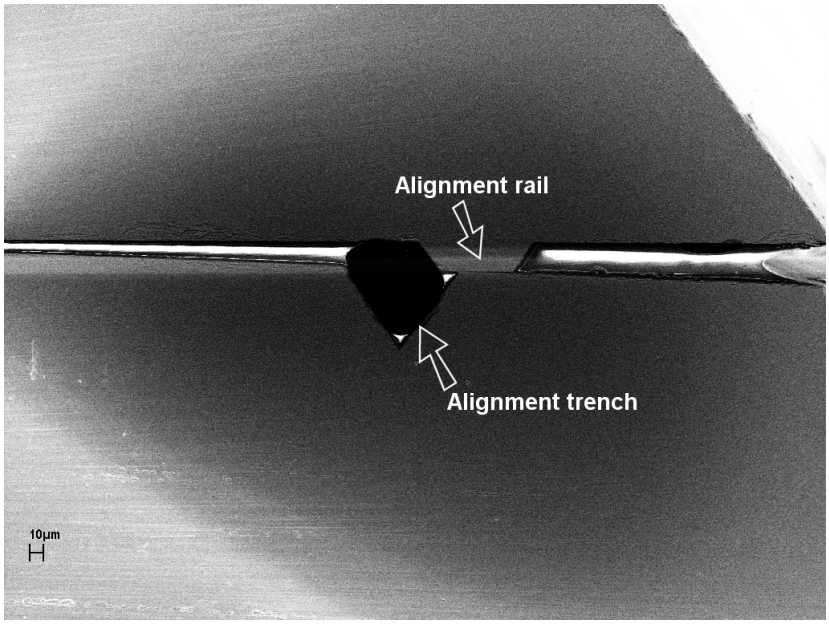
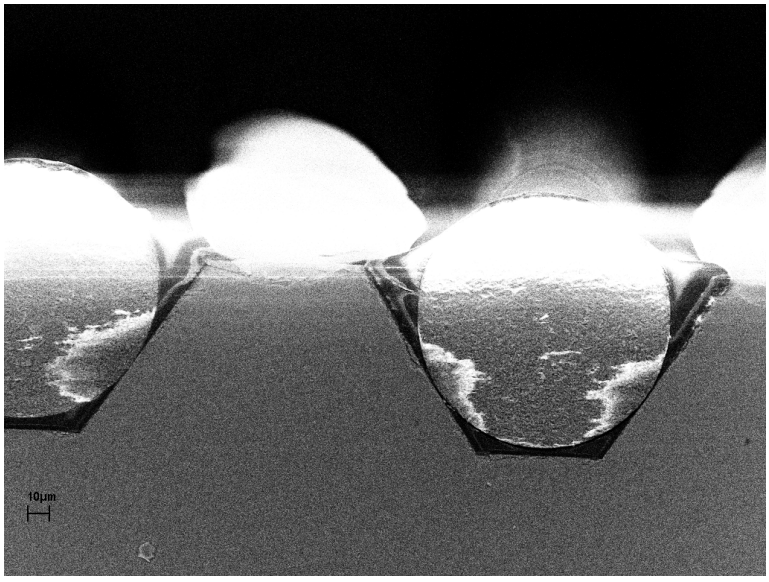
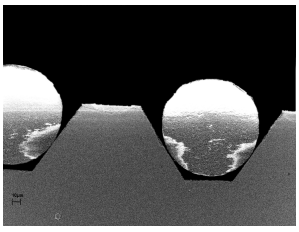


Figure 9.3: SEM picture of a misaligned alignment rail.

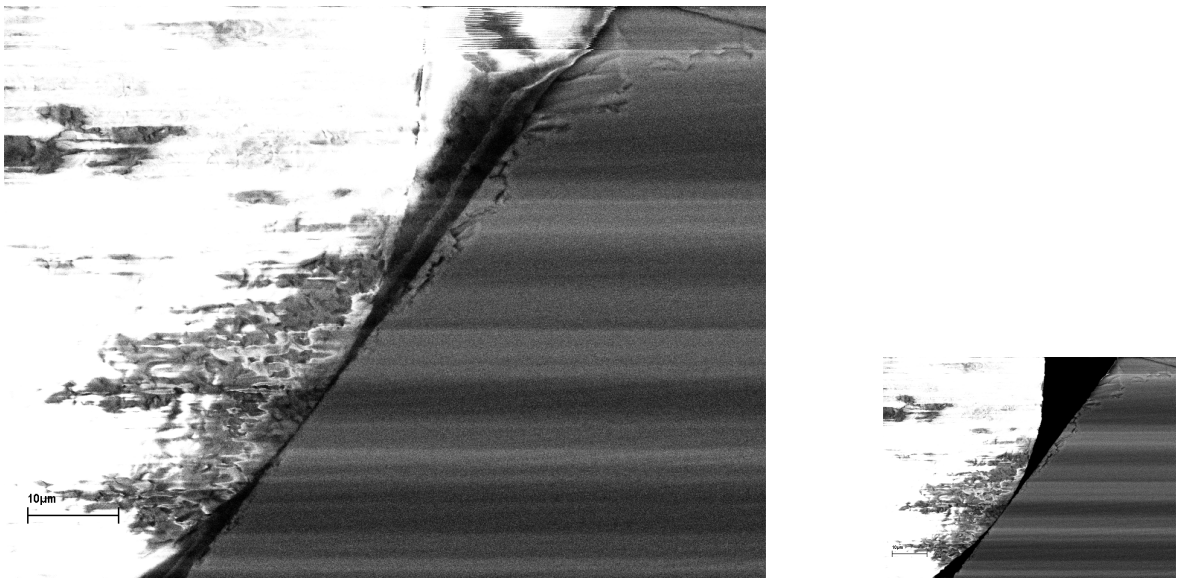


(a) Original photo



(b) Charging removed

Figure 9.4: SEM picture of the mounted optical fibers in the V-grooves.



(a) Original photo

(b) Charging removed

Figure 9.5: An optical fiber touching the side wall of the V-groove.

9.2 Mounting of waveguide part

After assembly of the fiber array and the top plate the waveguide chip is attached. An adhesive is used to attach the parts. Some of the adhesive will be applied in the gap between the fiber array and the waveguide chip. The refractive index of the adhesive is important, since it will affect the Fresnel reflection as described in section 4.2.

Three different adhesives have been used in the mounting process: An epoxy from Epotek (OG198), an acrylate from Ablestik (Luxtrak 4027), and an acrylate from Loctite (Loctite 382). OG198 is a low viscosity adhesive (100 cps) with a refractive index of 1.522 at 589 nm. Luxtrak 4027 is a high viscosity adhesive (1500 cps) with a refractive index of 1.57 at 589 nm. No specifications of Loctite 382 has been required, but the viscosity is high. OG198 and Luxtrack 4027 are cured by UV-exposure, while Loctite 382 is cured with an activator (Loctite 7455).

Only the two first adhesives are used in the light path. Both adhesives have a refractive index larger than 1.5, which is larger than the refractive indices of the waveguide and fiber core. The refractive indices are specified at 589 nm and not 1550 nm. Specifications of the refractive indices are not available at 1550 nm. Commercial available adhesives with a matched refractive index is difficult to find, since most pigtailing companies develope their own adhesive. The large refractive index will affect the Fresnel reflection, but can be used to demonstrate the pigtailing method.

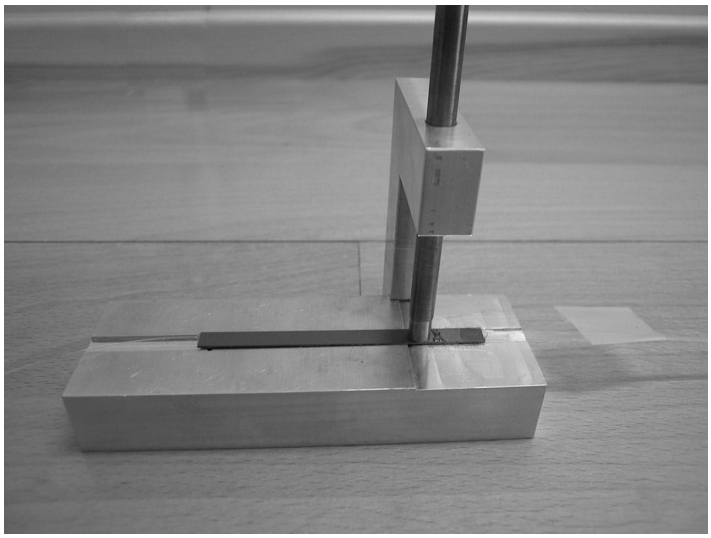
9.2.1 Mounting process

Before the assembly the waveguide chip is cleaned with isopropanol. An assembly tool is used to fix the waveguide chip with respect to the fiber array while gluing the samples together. A picture of the assembly tool is shown in figure 9.6. The assembly of the fiber array and the top plate is placed in the assembly tool with the alignment rails on the top plate facing upwards. The waveguide chip is placed carefully on top of the top plate with the waveguide side facing downwards. A rod is placed in the holder pressing on the waveguide chip. The waveguide chip is moved slightly side wards until the alignment rails reaches the alignment trenches. This can be quite difficult to determine, since the height of the alignment trenches only is 6 μm. It is important to assemble the parts rather carefully. Otherwise, corners of the alignment trench might break off during the assembly. A SEM picture of an alignment trench after an attempt to assemble the samples is shown in figure 9.7. It can be seen that some parts of the alignment structures are broken of. Glass broken of the alignment trenches during the assembly could be left in the bottom of the trench, which might influence on the alignment accuracy and should hence be avoided.

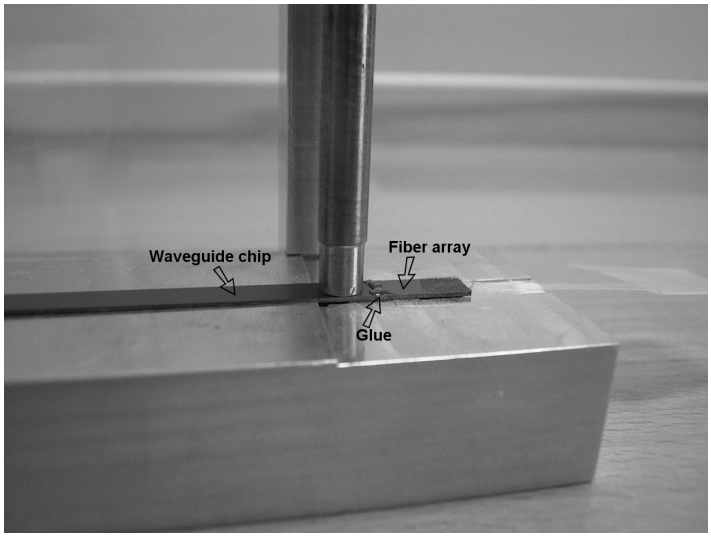
To ease the assembly between the waveguide chip and the top plate a design change is suggested. If the alignment trench is broader at the waveguide facet and slowly narrows down to the correct width, it will be easier to establish the correct position without ruining the alignment structures.

In the first assembly experiments the used adhesive was Epotek OG198, i.e. the same as used in assembly of the fiber array and top plate. While the assembly is placed in the holder, adhesive is dispensed and cured at the crossing between the waveguide chip and the fiber array. The pigtailed sample is subsequently removed from the holder and adhesive is dispensed between the fiber ends and the waveguide facet and finally cured. After the assembly the mounted sample was diced through to investigate the alignment accuracy in a back plane optical microscope. Two SEM pictures of the alignment structures are shown in figure 9.8 and 9.9. In figure 9.8 it can be seen that the alignment rail is placed within the alignment trench. However, the edges of the alignment trench do not touch the sides of the alignment rail. Instead the alignment trench is filled with adhesive. In figure 9.9 the alignment rail is totally misaligned not even reaching the alignment area, but is placed on top of the top cladding. The figure shows that it can be difficult to determine if the samples are properly aligned during the assembly process.

Most of the assembly experiments did look like figure 9.8. Two conditions could cause this misalignment. Either a fault (design or processing) making the alignment rail not fit correctly into the alignment trench or the misalignment is caused by the adhesive dispense and curing. To investigate which of the conditions described above causes the problem light has to be transmitted trough the waveguide during the assembly process. The measurements of loss during the assembly process are described in subsection 9.2.2.



(a) Total view



(b) Close-up

Figure 9.6: Assembly tool used to assemble the waveguide chip to the fiber array and top plate.

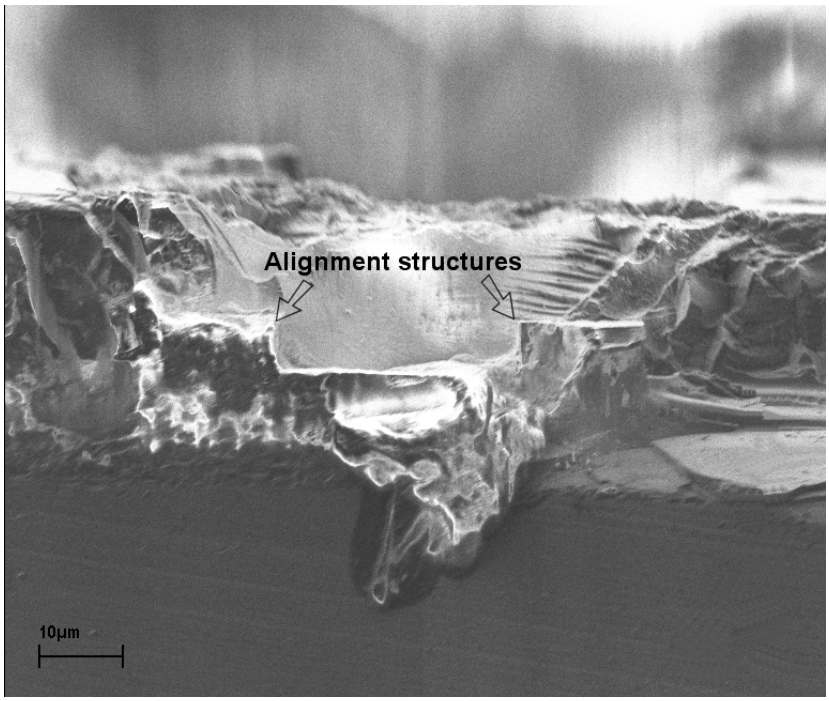
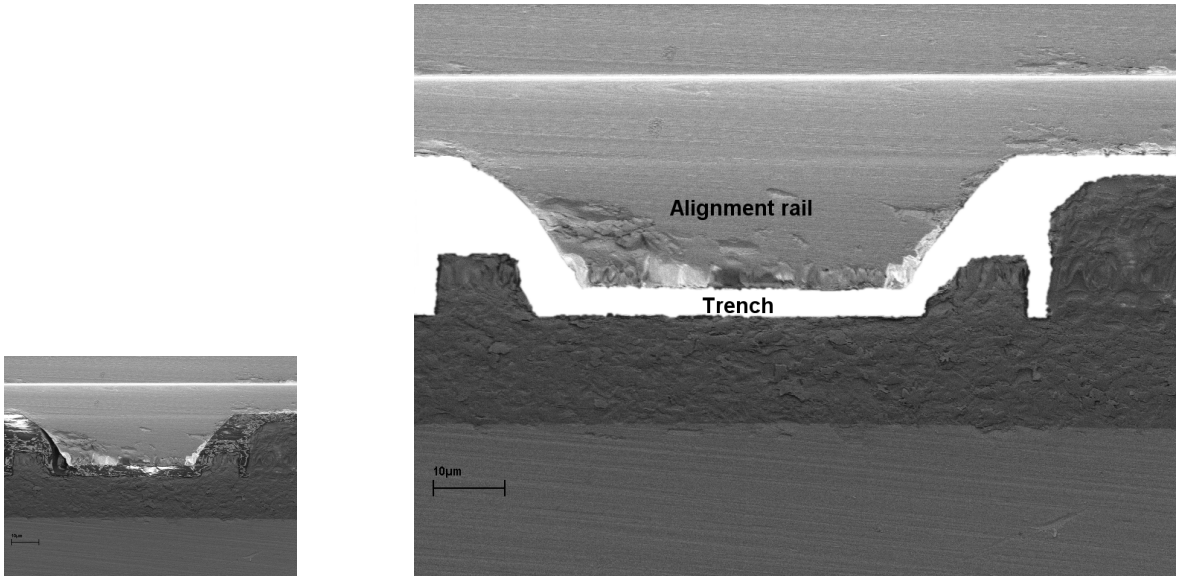


Figure 9.7: SEM picture of an waveguide alignment trench.



(a) Original photo

(b) Adhesive removed

Figure 9.8: A correctly positioned alignment rail in the waveguide alignment trench.

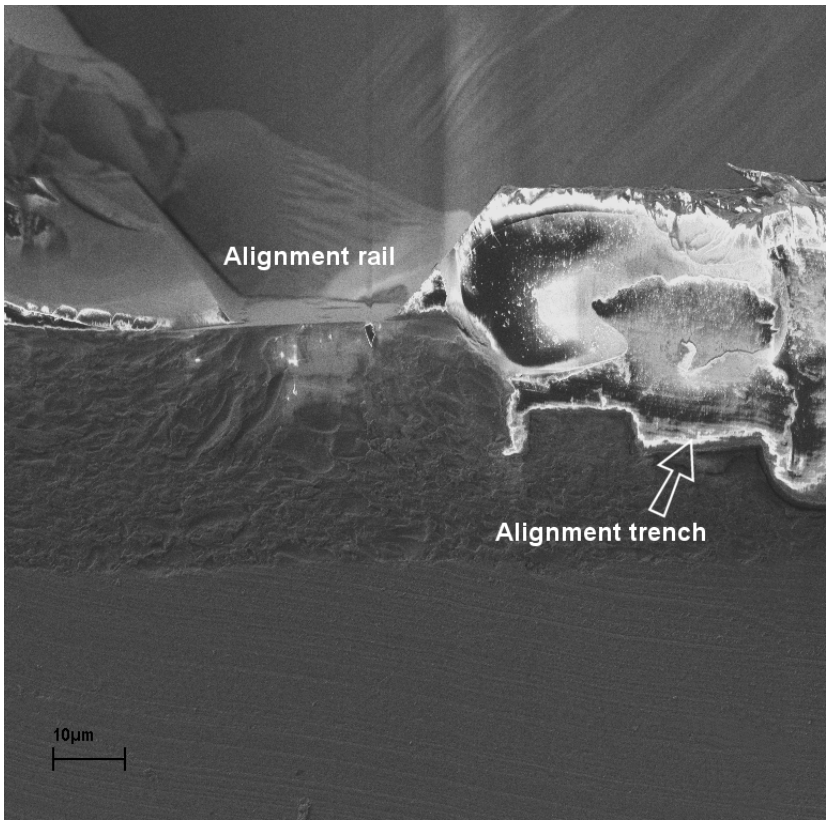


Figure 9.9: A misaligned alignment rail.

9.2.2 Loss Measurements during assembly

As stated in the last subsection it is necessary to track down the problem in the waveguide assembly process by transmitting light through the component. To measure the insertion loss during the assembly process an optical fiber is attached at the output side of the waveguide chip. The attachment of the optical fiber is done on the standard setup used for measuring the waveguides insertion loss (IL) and polarization dependent loss (PDL) as described in section 6.2.

The position of the output fiber is optimized by maximizing the light throughput. No index oil (on the output fiber side) is used during the measurement since this would affect the curing ability of the adhesive. After optimization of the position a tiny drop of Loctite 382 is placed on the fiber end. This affects the position of the fiber, which has to be re-optimized. The fiber is placed as close as possible to the waveguide facet. This is done to minimize the movement of the fiber during curing of the adhesive. An activator Loctite 7455 is sprayed onto the adhesive curing it within few seconds. The stability of the attachment is made stronger by repeating the gluing process three to four times. Each time only a small drop of adhesive is used. The reason for using small drops of adhesive is to minimize the movement of the optical fiber during the curing process. However, the fiber will move away from the optimal position. Hence, the insertion loss will increase during the process. Before dismounting the waveguide chip from the setup the insertion loss and the polarization dependent loss are measured.

An ASE light source is used to monitor the insertion loss during the assembly. All measurements are done at 1500 nm with an optical spectrum analyzer. The polarization dependency of the insertion loss is not determined during assembly.

Epotek OG198: The first assembly while monitoring the insertion loss is done with the adhesive Epotek OG198. This is the same adhesive as used in assembly of the fiber array. After assembly of the three parts in the holder an insertion loss of 12 dB is measured. The insertion loss after attaching the output fiber was 9 dB. Hence, an extra loss of 3 dB is occurring due to misalignment in the assembly. When dispensing and curing the adhesive the insertion loss is increased with approximately 30 dB. Hence, it is obvious that the adhesive is penetrating in between the top plate and the waveguide sample and hereby causes a misalignment of the waveguide chip with respect to the optical fiber.

Loctite 382 and Epotek OG198: To minimize the movement of the samples during the gluing process a adhesive with a larger viscosity is used to attach the samples in the holder. The chosen adhesive is Loctite 382, which is cured with an activator. Epotek OG198 is still used between the fiber ends and the waveguide chip. The measured insertion losses are listed in table 9.1. The assembly loss is 2.5 dB. Another 3.8 dB loss occurs in the gluing process. When post baking the Epotek OG198 on the hot plate after UV-curing is was observed, that the Loctite 382 is not stable at 150 $^{\circ}$C. Hence, it is not an appropriate choice of adhesive. After the post bake the total insertion loss caused by the pigtailing process was measured to 11.1 dB.

Luxtrak 4027 and Epotek OG198: Since the Loctite 382 adhesive did not function well another pigtailing attempt was made. The chosen adhesive is Luxtrak

	IL dB	**PDL dB**	**Excess Loss dB**
Before pigtailing	3.95	0.03	-
After gluing of output fiber	7.6	0.2	-
After assembly	10.1	-	2.5
Gluing and curing 1. time[1]	10.5	-	2.9
Gluing and curing 2. time[1]	10.7	-	3.1
Gluing and curing 3. time[1]	10.1	-	2.5
Gluing and curing 4. time[1]	12.9	-	5.3
Out of holder	12.7	-	5.1
Gluing between fiber and waveguide facet[2]	13.9	-	6.3
After dismounting output fiber	15.1	0.4	11.1

Table 9.1: Measured insertion loss during the pigtailing process. The used adhesives are Loctite 382[1] and Epotek OG198[2].

4027, which is an UV-curable adhesive with a viscosity of 1500 cps. The measured insertion losses during the pigtailing process are listed in table 9.2. The waveguide chip, where the input side was pigtailed in the last experiment, was used in this experiment to pigtail the output side. No extra loss can be determined for the assembly process since the measured value is within the PDL range of the component. In total 1.2 dB extra loss is obtained in the gluing process. This is a large improvement compared to the previous experiments. The adhesive fills the air gap between the optical fiber and the waveguide facet with a material having a refractive index closer to the refractive index of the glass. Hence, it should be possible to decrease the insertion loss in the gluing process instead of increasing it.

Unfortunately the optical fiber broke during the handling of the pigtailed component after the assembly. The break is close to the fiber array and it is impossible to splice a new fiber to the assembly. Hence, the polarization dependent loss after pigtailing is not measured. It remains to be emphasized that the experiment showed a good alignment between the waveguide sample and the fiber array.

Luxtrak 4027: Finally, two experiments were carried out with Luxtrak 4027 used as an adhesive both on the backside of the assembly and between the fiber ends and the waveguide facet. The measured insertion losses are listed in table 9.3 and 9.4. For both the samples the insertion loss decreased with 1.4 dB and 6.7 dB respectively during the gluing process. This emphasizes that the viscosity is an important factor when choosing the adhesive. Furthermore, it predicts that it is possible to maintain the good alignment of the substrates during the gluing process. The assembly of the two experiments were however not perfect. Especially with the high-delta waveguides (table 9.4). When inspecting the alignment trenches in an optical microscope some particles were observed in the trenches. This indicates that the buffer etch of the top cladding was to short and parts of the top cladding still remain in the alignment trenches. This would cause a misalignment as observed in the assembly process.

In conclusion, it remains to be emphasized, that three result can be drawn from the

	IL dB	**PDL dB**	**Excess Loss dB**
After pigtailing of input fiber	15.1	0.4	-
After assembly	15.4	-	0.3
Gluing and curing 1. time[1]	15.04	-	-0.06
Gluing and curing 2. time[1]	15.92	-	0.82
Gluing and curing 3. time[1]	15.75	-	0.65
Gluing and curing 4. time[1]	15.57	-	0.47
Out of holder	15.62	-	0.52
Gluing between fiber and waveguide facet[2]	16.32	-	1.22

Table 9.2: Measured insertion loss during the pigtailing process. The used adhesives are Luxtrak 4027[1] and Epotek OG198[2].

	IL dB	**PDL dB**	**Excess Loss dB**
Before pigtailing	4.4	0.3	-
After gluing of output fiber	7.7	0.6	-
After assembly	14.9	-	7.2
Gluing and curing 1. time	14.1	-	6.4
Gluing and curing 2. time	13.9	-	6.2
Gluing and curing 3. time	14.2	-	6.5
Gluing and curing 4. time	14.1	-	6.4
Gluing and curing 5. time	14.0	-	6.3
Out of holder	14.1	-	6.3
Gluing between fiber and waveguide facet	13.5	-	5.8

Table 9.3: Measured insertion loss during the pigtailing process. The used adhesive is Luxtrak 4027.

	IL dB	**PDL dB**	**Excess Loss dB**
Before pigtailing	0.47	0.05	-
After gluing of output fiber	1.21	0.12	-
After assembly	36.2	-	35.0
Gluing and curing 1. time	36.2	-	35.0
Gluing and curing 2. time	30.9	-	29.7
Gluing and curing 3. time	30.5	-	29.3
Gluing and curing 4. time	29.5	-	28.3
Gluing between fiber and waveguide facet	29.5	-	28.3

Table 9.4: Measured insertion loss during the pigtailing process. The used adhesive is Luxtrak 4027.

experiments. First, it has been shown that the alignment structures works perfectly fine and it is possible to align the two samples without using actively optimization of the position of the fiber array. Secondly, it is shown that the gluing process can be optimized to decrease the insertion loss during the process. Furthermore, the viscosity of the adhesive is an important feature when selecting an adhesive. The best result with the explored pigtailing process is an extra loss of 1.2 dB caused by the gluing process.

9.3 Summary

In this chapter the pigtailing process is described in details. The assembly of the fiber array and the top plate is done with a high alignment accuracy of both the alignment structures and the optical fibers. The assembly of the waveguide chip to the fiber array and top plate was found to be more troublesome. However, it have been shown that both a good alignment accuracy and a gluing process which decreased the insertion loss after assembly are possible. The best pigtailed component has an extra insertion loss of 1.2 dB due to the gluing process.

Chapter 10

Conclusion

This present thesis addresses research on pigtailing of planar waveguide components and is a part of the requirements to obtain the Ph.D. degree. The thesis includes development of a passive alignment method consisting of three parts: A waveguide chip with alignment trenches, a fiber array with alignment trenches, and a top plate with alignment rails used to assemble the parts at the correct position. Especially, the fabrication methods to obtain a low cost process have been explored. Furthermore, prototypes of a silicon motherboard to pigtail a laser diode and a Variable Optical Attenuator have been implemented.

A prototype of a silicon motherboard to pigtail a laser diode passively is realized. The method is derived from a method found in the literature. An improvement is proposed so the alignment accuracy does not depend on the alignment accuracy of the photolithography process. The improved fabrication process is presented and it has been shown that the motherboard can be fabricated.

A prototype of a Variable Optical Attenuator (VOA) is designed and realized. Three different designs of the splitter regions have been implemented. It has been shown that the design has an influence of the amount of keyholes in the top cladding. The VOA based on a tapered splitter showed a high amount of keyholes. Measurements of the fabricated components showed a high insertion loss and polarization dependent loss. This is caused by using a production process optimized to a larger refractive index difference between the core and the cladding. Hence, raising the refractive index of the core would easily solve the problem. The extinction ratio of the components was measured to around -40 dB, which gives the components a really high attenuation level. The wavelength dependency of the extinction ratio was small.

A new passive pigtailing method for planar waveguide components has been proposed. In the development process the advantages from other pigtailing methods have been implemented in the new method. The advantages of the method are: The ability of testing the planar waveguide components before pigtailing and packaging. The waveguide structures and the alignment trenches are defined in the same photolithography steps. Also the V-grooves and alignment trenches on the fiber array carrier are defined in one photolithography step. Using one photolithography step provides a good horizontal alignment accuracy without the need of a high precision photolithography

process. The use of simultaneously etched V-grooves and alignment trenches allows for a systematic offset of the line width while maintaining the optical alignment. This is due to the fact that the fiber core and the alignment position of the alignment rail move together vertically, maintaining their relative alignment. Finally, but not the least, the cost of the processing has been in focus in the development process. All long expensive single wafer processes have been avoided and if possible a batch process has been chosen.

Planar waveguide components integrated with alignment trenches have been fabricated. It has been shown that the use of a LPCVD polysilicon etch mask causes a lower roughness of the etched structures than a sputtered amorphous silicon mask. Components with low insertion loss and low polarization dependent loss have been realized. Furthermore, it has been demonstrated that the extra processing necessary to fabricate the alignment trenches does not influence on the waveguide performance.

A method to align the mask pattern for the potassium hydroxide (KOH) etch to the crystal plane of the silicon substrate has been implemented. The accuracy of the alignment is within 0.05°.

To fabricate the V-groove array and the top plate a nitride mask has been used as etch mask in KOH. Due to the etch characteristics of the KOH etch it is important to stop the mask etch at the interface between the nitride layer and the silicon wafer. Etching non-uniform into the silicon substrate will affect the line width of the etched structures and hence alter the alignment precision. Therefore the uniformity of the etch rate in the nitride etch is important. An etch process of nitride by RIE by a SF_6 - O_2 plasma has been explored. The uniformity of the etch rate has been investigated with respect to different process parameters. It has been shown that the process parameters do have an influence of the uniformity of the etch rate. The lowest etch rate uniformity obtained was measured to 10 %. However, this was not considered to be low enough for this purpose. Instead a wet-etch in phosphoric acid was used to etch the nitride mask. The phosphoric acid has a high selectivity between nitride and silicon, which solves the problem with etching into the silicon substrate. Another advantage with the use of a wet-etch is that it is a batch process. Hence, the solution is cheaper than etching single wafers by RIE.

After completed fabrication the line widths of the structures have been determined. The standard deviation of the width of the V-grooves on one chip is measured to 0.15 μm. The standard deviation of the width of the alignment trenches is 0.05 μm, and the standard deviation of the width of the alignment rails is 0.1 μm. The standard deviation of the misalignment in the total pigtailing process is calculated to 0.17 μm. It has been shown that the fabrication process is accurate enough to be used in the pigtailing process.

To obtain a low coupling loss between the optical fiber and the planar waveguide the facet of the waveguide chip has to be smooth. This is commonly obtained by polishing the waveguide facet. To lower the need for polishing the dicing process has been investigated. Both the blade type and the dicing parameters have an influence on the dicing quality. Changing the dicing blade to a resinoid diamond blade and optimizing the dicing process have resulted in a large improvement of the smoothness

of the waveguide facet. Furthermore, cracking of the top and bottom of the diced chips has been minimized.

A setup and procedure for polishing of the waveguide facet have been implemented. The procedure gives a very smooth surface when polishing a chip with buffer layer. However, when polishing a waveguide chip, it has been seen that the top cladding chips off. Alternating the first step in the polishing process has decreased the amount of chipping. It is expected that chipping of the top cladding can be avoided by a further optimization of the step. Since the quality of the diced facet is really smooth, the waveguide chips have been used for pigtailing without polishing of the facets.

The processed waveguide chips have been assembled and the pigtailing method has been evaluated. First step of the process is an assembly of the fiber array carrier, the optical fibers, and the top plate. It has been shown that both the optical fibers and the alignment rail are positioned correctly during the assembly. The waveguide chip has been attached to the fiber array and top plate with different kind of adhesives. It has been shown that an adhesive with a low viscosity will make the parts move with respect to each other, probably due to capillary forces. An adhesive with a higher viscosity improved the gluing process. Instead of an increase of the loss during the gluing process the loss decreased. A decrease of the loss is to be expected, since the air gap between the fiber end and the waveguide facet is filled with a refractive index matched media. An assembly was made with no measurable excess loss. Hence, it has been shown that the alignment structures work as proposed. The lowest pigtailing loss, due to the gluing process, was measured to 1.2 dB.

The developed pigtailing method and the measurements of the pigtailed components show very encouraging results. It has been shown that the alignment technique works, even though the gluing process needs further investigations. The alignment precision is obtained by the alignment structures on each of the three parts. Which makes it suitable for mass production of components. A major part of the processing, involved in the method, is based on batch processing, which potential makes it a low cost method. Another advantage of the method is, that the waveguide chip may be tested before pigtailing. The market is focused on components with a high level of functionality and hereby high cost. Hence, it might be profitable to determine the quality of the components before pigtailing.

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Appendix A

Silicon motherboard process list

Appendix A is only available to supervisors and censors.

Appendix B

Mask calculations

Calculations on the width of the fiber V-groove, V-groove alignment trench and top plate alignment rail are described below. A detailed description of the pigtailing process is given in chapter 5. The whole processing sequence is listed in Appendix C. In section B.1 the calculations on the masks for the fiber array are described. In section B.2 the calculations of the masks for the top plate are described.

B.1 Fiber array

In the processing of the fiber array both the alignment trenches and the V-grooves are defined in the same processing step. The width of these are determined below.

B.1.1 V-groove

In figure B.1 the cross section of the V-groove with an optical fiber is shown. On the figure the geometry of the system is shown. The key parameters are as follows:

- r = radius of fiber
- d = distance from silicon surface to the center of the fiber
- θ = angle of the KOH etched structures defined by crystallographic planes
- w = width of the V-groove
- h = height of the V-groove

Using trigonometric functions for a right triangle in figure B.1, it can easily be shown that[32]:

$$\begin{aligned} \sin(\theta) &= \tfrac{r}{h-d} \\ \Updownarrow & \\ h &= \tfrac{r}{\sin(\theta)} + d \end{aligned} \tag{B.1}$$

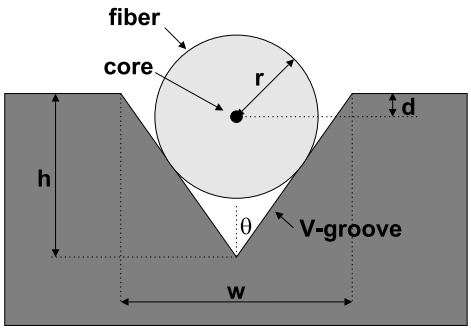

Figure B.1: Schematic of an optical fiber positioned in a KOH-etched V-groove.

and

$$\begin{aligned} \tan(\theta) &= \tfrac{w}{2h} \\ \Updownarrow & \\ h &= \tfrac{w}{2\tan(\theta)} \end{aligned} \tag{B.2}$$

Combining the two equations gives that the width of the V-groove can be determined as follows:

$$\begin{aligned} \tfrac{w}{2\tan(\theta)} &= \tfrac{r}{\sin(\theta)} + d \\ \Updownarrow & \\ w &= 2\tan(\theta)(\tfrac{r}{\sin(\theta)} + d) \end{aligned} \tag{B.3}$$

The angle θ is defined by crystallographic considerations to be 35.26 $^\circ$ [38]. The radius of an optical fiber is 62.5 μm. It has been chosen that the distance from the middle of the fiber core to the silicon surface d = 18.3 μm. This way the surface of the silicon wafer and the surface of the waveguide substrate are around the same height assembling the component. Given these numbers the width of the fiber V-groove is calculated to 179.0 μm.

An offset of the width of the V-groove Δw would cause an offset in the position of the center of the optical fiber Δd. From equation B.3 the relation between the two offset is derived to

$$\Delta w = 2\tan(\theta)\Delta d \tag{B.4}$$

If the width of the V-groove is 0.5 μm too small it would correspond to a 0.35 μm upwards shift the the center of the optical fiber.

B.1.2 Alignment trench

In figure B.2 the cross section of the V-groove alignment trench and the top plate alignment rails is shown. The key parameters are as follows:

- x = distance between waveguide alignment trenches
- θ = angle of the KOH etched structures defined by crystallographic planes
- w' = width of alignment trench

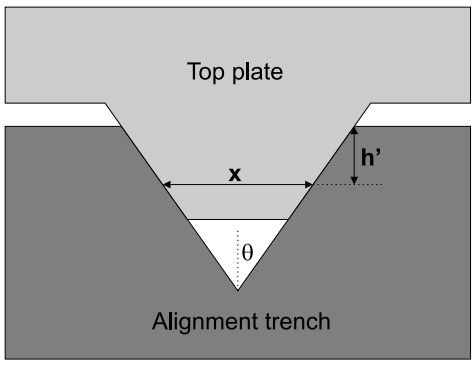

Figure B.2: Schematic of an alignment rail positioned in a KOH-etched alignment trench.

- h' = height of alignment trench

Using the trigonometric functions for a right triangle it can be shown that:

$$\begin{aligned} \tan(\theta) &= \tfrac{w'-x}{2}\tfrac{1}{h'} \\ \Updownarrow & \\ w' &= x + 2h'\tan(\theta) \end{aligned} \tag{B.5}$$

The distance between the waveguide alignment trenches x is set to 15, 30 and 60 μm respectively. On the waveguide substrate this distance is at the top of the waveguide core. The middle of the optical fiber is set to be 18.3 μm below the silicon surface. The height of the waveguide core is 6 μm. A thin silica layer of 0.3 μm is deposited on the top of the waveguides before etch. Hence, the height of the alignment trench should be 3.3 μm lower than the distance from the silicon surface to the middle of the optical fiber. Then the middle of the waveguide core will be aligned to the middle of the optical fiber. Hereby, the height of the alignment trench h' is determined to 15 μm. Given these numbers the widths of the alignment trench w' are determined to 36.2, 51.2 and 81.2 μm, respectively. An offset of the width of the alignment trench would cause a shift of the placement of the alignment rail. The shift can be calculated by equation B.4 due to the similarities with the fiber V-groove.

B.2 Top plate masks

The processing of the top plate substrate have two masks. The first mask is used to fabricate the alignment rails. The second mask is a backside mask. The wafer is etched from the backside through the whole wafer. This is done to ensure room for the optical fibers on the fiber array in the assembly of the pigtailing parts. The width of the alignment rails and the width of the backside pattern are described below.

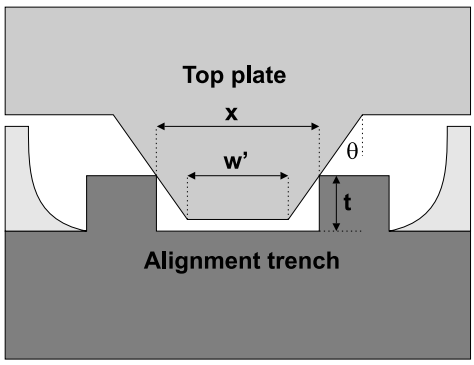

Figure B.3: Schematic of an alignment rail positioned in a waveguide alignment trench.

B.2.1 Alignment rails

In figure B.3 the cross section of the waveguide alignment trench and the top plate alignment rails is shown. The key parameters are as follows:

- x = distance between waveguide alignment trenches
- θ = angle of the KOH etched structures defined by crystallographic planes
- w'' = width of alignment rail
- h'' = height of waveguide alignment trench

Using the trigonometric functions for a right triangle, it can be shown that

$$\begin{aligned} \tan(\theta) &= \frac{x-w''}{2}\frac{1}{h''} \\ \Updownarrow & \\ w'' &= x - 2h''\tan(\theta) \end{aligned} \tag{B.6}$$

The distance between the alignment trenches x have been chosen to be 15, 30 and 60 μm respectively. The etch depth of the waveguide cores is 6.8 μm. However, the alignment rails should not touch the bottom of the alignment trenches. Hence, the distance h'' is set to 5.0 μm. This ensures that the alignment rails will be stopped by the upper part of the alignment trench not the bottom. Given these numbers the widths of the alignment rails w'' are calculated to 7.9, 22.9 and 52.9 μm, respectively.

An offset of either the width of the waveguide trench or the width of the alignment rail could cause the alignment rail to touch the bottom of the alignment trench instead of the upper edges. The 1.8 μm space to the bottom of the alignment trench correspond to an offset of the width of 1.3 μm (equation B.4).

B.2.2 Backside mask

In figure B.4 the geometry of the top plate is shown. The key parameters are as follows:

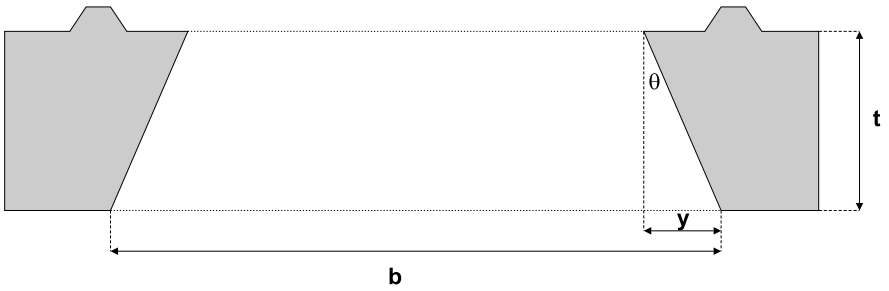

Figure B.4: Schematic of the cross section of a top plate.

- θ = angle of the KOH etched structures defined by crystallographic planes
- t = thickness of the silicon wafer
- y = distance
- b = width of backside pattern

Using the trigonometric functions it can be shown that:

$$\begin{aligned} \tan(\theta) &= \frac{y}{t} \\ \Updownarrow & \\ y &= t\tan(\theta) \end{aligned} \tag{B.7}$$

Hence, y is determined by the thickness of the silicon wafer and the angle of the KOH etched structure. The thickness of the used silicon wafers are 525 ± 25 μm. To ensure that the width is large enough t is set to 550 μm.

The reason for etching through the whole silicon wafer is the ensure room for the optical fibers. There are 11 fibers between the two alignment trenches. Consequently, the width of the backside pattern can be determined by:

$$\begin{aligned} b - 2y &= 10d' + 2r \\ \Updownarrow & \\ b &= 10d' + 2r + 2t\tan(\theta) \end{aligned} \tag{B.8}$$

where d' is the distance between the optical fibers and r is the radius of the optical fiber.

The distance between the optical fibers d' is set to 250 μm and the radius of the optical fiber r is 62.5 μm. Given these numbers the width of the backside pattern b is calculated to 3403 μm. The dimensions of the backside mask are not critical. Even an width offset above 20 μm would not cause a problem.

Appendix C

Pigtailing method process list

Appendix C is only available for supervisors and censors.